ANNA UNIVERSITY, CHENNAI
UNIVERSITY DEPARTMENTS
REGULATIONS - 2019
M.E. VLSI DESIGN
CHOICE BASED CREDIT SYSTEM

VISION

The Department of ECE shall strive continuously to create highly motivated, technologically competent engineers, be a benchmark and a trend setter in Electronics and Communication Engineering by imparting quality education with interwoven input from academic institutions, research organizations and industries, keeping in phase with rapidly changing technologies imbibing ethical values.

MISSION

- Imparting quality technical education through flexible student centric curriculum evolved continuously for students of ECE with diverse backgrounds.
- Providing good academic ambience by adopting best teaching and learning practices.
- Providing congenial ambience in inculcating critical thinking with a quest for creativity, innovation, research and development activities.
- Enhancing collaborative activities with academia, research institutions and industries by nurturing ethical entrepreneurship and leadership qualities.
- Nurturing continuous learning in the stat-of-the-art technologies and global outreach programmes resulting in competent world class engineers.

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PROGRAMME EDUCATIONAL OBJECTIVES:

1. Teach students to understand the principles involved in the latest hardware and software required for designing and critically analyzing electronic circuits relevant to industry and society
2. Blend theory and laboratory to make students appreciate the concepts in the working of electronic circuits
3. Mould students to progress and develop with ethics and to communicate effectively
4. Motivate students to take up socially relevant and challenging projects and propose innovative solutions to problems for the benefit of the society
5. To motivate students to become entrepreneurs to develop indigenous solutions.

PROGRAM OUTCOMES:

PO#	Graduate Attribute	Programme Outcome
1.	Research aptitude	An ability to independently carry out research /investigation and development work to solve practical problems
2.	Technical documentation	An ability to write and present a substantial technical report/document
3.	Technical competence	Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program
4.	Engineering Design	An ability to apply various advanced tools and techniques to develop efficient Hardware solutions
5.	The engineer and society	Apply technical knowledge towards the development of socially relevant products
6.	Environment and sustainability	Ensure development of eco friendly indigenous products.

MAPPING OF PROGRAMME EDUCATIONAL OBJECTIVES WITH PROGRAMME OUTCOMES:

A broad relation between the programme objective and the outcomes is given in the following table:

PEOs	Programme Outcomes					
	PO1	PO2	PO3	PO4	PO5	PO6
I.	√	√	√	√		
II.	√	√	√	√		
III.		√				
IV.					√	√
V.	√	√	√	√	√	√

YEAR	SEMESTER	COURSE TITLE	PO1	PO2	PO3	PO4	PO5	PO6
YEAR 1	SEMESTER 1	Advanced Applied Mathematics				✓	✓	
		Digital CMOS VLSI Design	3		3	2	1	1
		Analog Integrated Circuit Design	✓		✓	✓		✓
		ASIC Design	3		3	2	1	1
		Research Methodology and IPR						
		Audit Course - I						
		Analog and Digital CMOS VLSI Design Laboratory	3	1	3	3	2	2
		Printed Circuit Board Design and Component Assembling Laboratory		1	3	3	2	1
	SEMESTER 2	Embedded System Design	1	2	1	2	3	3
		Low Power VLSI Design	✓		✓	✓		✓
		Statistical Signal Processing	3		3	2	1	1
		Program Elective II	✓		✓	✓		✓
		Program Elective III	✓		✓	✓		✓
		Audit Course - II						
		Embedded Systems and Robotics Laboratory	1		2	3	1	3
		Signal Processing and RTL Synthesis Laboratory	✓	✓	✓	✓	✓	✓
		Mini Project with Seminar	✓	✓	✓	✓	✓	✓
YEAR 2	SEMESTER 3	Program Elective IV	✓		✓	✓		✓
		Program Elective V	✓		✓	✓		✓
		Program Elective VI	✓		✓	✓		✓
		Open Elective (*one from the list of 6 Open Electives)	✓		✓	✓		✓
		Dissertation – I	✓	✓	✓	✓	✓	✓
	SEMESTER 4	Dissertation – II	✓	✓	✓	✓	✓	✓

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CHOICE BASED CREDIT SYSTEM
I - IV CURRICULA AND SYLLABI
M.E. VLSI DESIGN
SEMESTER I

S.No.	COURSE CODE	COURSE TITLE	CATEGORY	PERIODS PER WEEK			CONTACT PERIODS	CREDITS
				L	T	P		
THEORY								
1.	MA5159	Advanced Applied Mathematics	FC	3	1	0	4	4
2.	VL5152	Digital CMOS VLSI Design	PCC	3	0	0	3	3
3.	AP5151	Analog Integrated Circuit Design	PCC	3	0	0	3	3
4.	VL5151	ASIC Design	PCC	3	0	0	3	3
5.	RM5151	Research Methodology and IPR	RMC	2	0	0	2	2
6.		Audit Course – I*	AC	2	0	0	2	0
PRACTICALS								
7.	VL5161	Analog and Digital CMOS VLSI Design Laboratory	PCC	0	0	4	4	2
8.	AP5261	Printed Circuit Board Design and Component Assembling Laboratory	PCC	0	0	4	4	2
			TOTAL	**16**	**1**	**8**	**25**	**19**

* Audit Course is optional

SEMESTER II

S.No.	COURSE CODE	COURSE TITLE	CATEGORY	PERIODS PER WEEK			CONTACT PERIODS	CREDITS
				L	T	P		
THEORY								
1.	AP5152	Embedded System Design	PCC	3	0	0	3	3
2.	VL5251	Low Power VLSI Design	PCC	3	0	0	3	3
3.	AP5153	Statistical Signal Processing	PEC	3	0	0	3	3
4.		Program Elective I	PEC	3	0	0	3	3
5.		Program Elective II	PEC	3	0	0	3	3
6.		Audit Course – II*	AC	2	0	0	2	0
PRACTICALS								
7.	AP5161	Embedded Systems and Robotics Laboratory	PCC	0	0	4	4	2
8.	VL5261	Signal Processing and RTL Synthesis Laboratory	PCC	0	0	4	4	2
	VL5211	Mini Project with Seminar	EEC	0	1	2	3	2
			TOTAL	**17**	**1**	**10**	**28**	**21**

* Audit Course is optional

SEMESTER III

S.No.	COURSE CODE	COURSE TITLE	CATEGORY	PERIODS PER WEEK			CONTACT PERIODS	CREDITS
				L	T	P		
THEORY								
1.		Program Elective III	PEC	3	0	0	3	3
2.		Program Elective IV	PEC	3	0	0	3	3
3.		Program Elective V	PEC	3	0	0	3	3
		Open Elective	OEC	3	0	0	3	3
PRACTICALS								
4.	VL5311	Dissertation – I	EEC	0	0	12	12	6
			TOTAL	**12**	**0**	**12**	**24**	**18**

SEMESTER IV

S.NO.	COURSE CODE	COURSE TITLE	CATEGORY	PERIODS PER WEEK			CONTACT PERIODS	CREDITS
				L	T	P		
PRACTICALS								
1.	VL5411	Dissertation – II	EEC	0	0	24	24	12
			TOTAL	**0**	**0**	**24**	**24**	**12**

TOTAL NO. OF CREDITS : 70

FOUNDATION COURSES (FC)

SI. NO	COURSE CODE	COURSE TITLE	CATEGORY	PERIODS PER WEEK			CONTACT PERIODS	CREDITS
				L	T	P		
1.	MA5159	Advanced Applied Mathematics	FC	3	1	0	4	4

PROGRAM CORE COURSES (PCC)

SI. NO	COURSE CODE	COURSE TITLE	CATEGORY	PERIODS PER WEEK			CONTACT PERIODS	CREDITS
				L	T	P		
1.	VL5152	Digital CMOS VLSI Design	PCC	3	0	0	3	3
2.	AP5151	Analog Integrated Circuit Design	PCC	3	0	0	3	3
3.	VL5151	ASIC Design	PCC	3	0	0	3	3
4.	VL5161	Analog and Digital CMOS VLSI Design Laboratory	PCC	0	0	4	4	2
5.	AP5261	Printed Circuit Board Design & Component Assembling Laboratory	PCC	0	0	4	4	2
6.	AP5152	Embedded System Design	PCC	3	0	0	3	3
7.	VL5251	Low Power VLSI Design	PCC	3	0	0	3	3
8.	AP5153	Statistical Signal Processing	PCC	3	0	0	3	3
9.	AP5161	Embedded Systems and Robotics Laboratory	PCC	0	0	4	4	2
10.	VL5261	Signal Processing and RTL Synthesis Laboratory	PCC	0	0	4	4	2

PROGRAM ELECTIVE COURSES (PEC)

S. NO	COURSE CODE	SUBJECTS	CATEGORY	PERIODS PER WEEK			CONTACT PERIODS	CREDITS
				L	T	P		
1.	AP5078	Wireless Sensor Networks	PEC	3	0	0	3	3
2.	AP5074	PCB Design And Fabrication	PEC	3	0	0	3	3
3.	AP5071	Advanced Microprocessors and Microcontrollers	PEC	3	0	0	3	3
4.	AP5072	Electronics for Solar Power	PEC	3	0	0	3	3
5.	AP5076	Robotics and Intelligent Systems	PEC	3	0	0	3	3
6.	AP5075	RF System Design	PEC	3	0	0	3	3
7.	AP5077	Signal Integrity for High Speed Design	PEC	3	0	0	3	3
8.	AP5073	EMI and EMC in System Design	PEC	3	0	0	3	3
9.	VL5001	Hardware and Software Co-design	PEC	3	0	0	3	3
10.	VL5002	Reconfigurable Computing	PEC	3	0	0	3	3
11.	VL5003	Evolvable Hardware	PEC	3	0	0	3	3
12.	VL5004	Power Management and Clock Distribution Circuits	PEC	3	0	0	3	3
13.	VL5005	Testing of VLSI Circuits	PEC	3	0	0	3	3
14.	VL5006	SoC Design	PEC	3	0	0	3	3
15.	VL5007	Data Converters	PEC	3	0	0	3	3
16.	VL5008	CAD for VLSI Circuits	PEC	3	0	0	3	3
17.	VL5009	VLSI Signal Processing	PEC	3	0	0	3	3
18.	AP5251	Advanced Digital System Design	PEC	3	0	0	3	3

OPEN ELECTIVE COURSES (OEC)

*(out of 6 courses one course must be selected)

SI. NO	COURSE CODE	COURSE TITLE	CATEGORY	PERIODS PER WEEK			CONTACT PERIODS	CREDITS
				L	T	P		
11.	OE5091	Business Data Analytics	OEC	3	0	0	3	3
12.	OE5092	Industrial Safety	OEC	3	0	0	3	3
13.	OE5093	Operations Research	OEC	3	0	0	3	3
14.	OE5094	Cost Management of Engineering Projects	OEC	3	0	0	3	3
15.	OE5095	Composite Materials	OEC	3	0	0	3	3
16.	OE5096	Waste to Energy	OEC	3	0	0	3	3

AUDIT COURSES (AC)

Registration for any of these courses is optional to students

SL. NO	COURSE CODE	COURSE TITLE	PERIODS PER WEEK			CREDITS
			Lecture	Tutorial	Practical	
1.	AX5091	English for Research Paper Writing	2	0	0	0
2.	AX5092	Disaster Management	2	0	0	0
3.	AX5093	Sanskrit for Technical Knowledge	2	0	0	0
4.	AX5094	Value Education	2	0	0	0
5.	AX5095	Constitution of India	2	0	0	0
6.	AX5096	Pedagogy Studies	2	0	0	0
7.	AX5097	Stress Management by Yoga	2	0	0	0
8.	AX5098	Personality Development Through Life Enlightenment Skills	2	0	0	0
9.	AX5099	Unnat Bharat Abhiyan	2	0	0	0
Total Credits						**0**

EMPLOYABILITY ENHANCEMENT COURSES (EEC)

SI. NO	COURSE CODE	COURSE TITLE	CATEGORY	PERIODS PER WEEK			CONTACT PERIODS	CREDITS
				L	T	P		
1.	VL5211	Mini Project with Seminar	EEC	0	1	2	3	2
2.	VL5311	Dissertation – I	EEC	0	0	12	12	6
3.	VL5411	Dissertation – II	EEC	0	0	24	24	12

	M.E VLSI DESIGN					
	SUBJECT AREA	**CREDITS PER SEMESTER**				**CREDITS TOTAL**
		I	**II**	**III**	**IV**	
1.	FC	4	-	-	-	**4**
2.	PCC	13	10	-	-	**23**
3.	PEC	-	9	9	-	**18**
4.	RMC	2	-	-	-	**2**
5.	OEC	-	-	3	-	**3**
6.	EEC	-	2	6	12	**20**
7.	Non Credit & Audit Course	✓	✓	-	-	**-**
	TOTAL CREDITS	**19**	**21**	**18**	**12**	**70**

MA5159 ADVANCED APPLIED MATHEMATICS L T P C
3 1 0 4

OBJECTIVES:

- To encourage students to develop a working knowledge of the central ideas of linear algebra.
- To enable students to understand the concepts of probability and random variables.
- To make students understand the notion of a Markov chain, and how simple ideas of conditional probability and matrices can be used to give a thorough and effective account of discrete-time Markov chains.
- To familiarize the students with the formulation and construction of a mathematical model for a linear programming problem in real life situation.
- To introduce the Fourier Transform as an extension of Fourier techniques on periodic functions and to solve partial differential equations.

UNIT I LINEAR ALGEBRA 12

Vector spaces – norms – Inner Products – Eigenvalues using QR transformations – QR factorization - generalized eigenvectors – Canonical forms – singular value decomposition and applications - pseudo inverse – least square approximations --Toeplitz matrices and some applications.

UNIT II ONE DIMENSIONAL RANDOM VARIABLES 12

Random variables - Probability function – moments – moment generating functions and their properties – Binomial, Poisson, Geometric, Uniform, Exponential, Gamma and Normal distributions – Function of a Random Variable.

UNIT III RANDOM PROCESSES 12

Classification – Auto correlation - Cross correlation - Stationary random process – Markov process –- Markov chain - Poisson process – Gaussian process.

UNIT IV LINEAR PROGRAMMING 12

Formulation – Graphical solution – Simplex method – Two phase method - Transportation and Assignment Models

UNIT V FOURIER TRANSFORM FOR PARTIAL DIFFERENTIAL EQUATIONS 12

Fourier transforms: Definitions, properties-Transform of elementary functions, Dirac Delta functions – Convolution theorem – Parseval‘s identity – Solutions to partial differential equations: Heat equations, Wave equations, Laplace and Poisson‘s equations.

TOTAL: 45+15=60 PERIODS

COURSE OUTCOMES:

At the end of the course, students will be able to

- Apply the concepts of linear algebra to solve practical problems.
- Use the ideas of probability and random variables in solving engineering problems.
- Classify various random processes and solve problems involving stochastic processes.
- Formulate and construct mathematical models for linear programming problems and solve the transportation and assignment problems.
- Apply the Fourier transform methods of solving standard partial differential equations.

REFERENCES:

1. Andrews, L.C. and Philips.R.L., “Mathematical Techniques for engineering and scientists”, Printice Hall of India, New Delhi, 2006.
2. Bronson, R., “Matrix Operation”, Schaum‘s outline series, Tata McGrawHill, New York, 2011.
3. O‘Neil P.V., “Advanced Engineering Mathematics”, Cengage Learning, 8th Edition, India, 2017.
4. Oliver C. Ibe, “Fundamentals of Applied Probability and Random Processes”, Academic Press, Boston, 2014.

5. Sankara Rao, K., “Introduction to partial differential equations”, Prentice Hall of India, pvt, Ltd, 3rd Edition, New Delhi, 2010.
6. Taha H.A., “Operations Research: An introduction”, Ninth Edition, Pearson Education, Asia, 10th Edition, New Delhi, 2017.

VL5152 DIGITAL CMOS VLSI DESIGN L T P C
3 0 0 3

OBJECTIVES:

- To introduce the transistor level design of all digital building blocks common to all CMOS microprocessors, network processors, digital backend of all wireless systems etc
- To introduce the principles and design methodology in terms of the dominant circuit choices, constraints and performance measures
- To learn all important issues related to size, speed and power consumption.

UNIT I MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER 12

MOS(FET) Transistor Characteristic under Static and Dynamic Conditions, MOS Transistor Secondary Effects, CMOS Inverter-Static Characteristic, Dynamic Characteristic, Power, Energy, and Energy Delay parameters, Stick diagram and Layout diagrams.

UNIT II COMBINATIONAL LOGIC CIRCUITS 9

Static CMOS design, Different styles of logic circuits, Logical effort of complex gates, Static and Dynamic properties of complex gates, Interconnect Delay, Dynamic Logic Gates.

UNIT III SEQUENTIAL LOGIC CIRCUITS 9

Static Latches and Registers, Dynamic Latches and Registers, Timing Issues, Pipelines, Nonbistable Sequential Circuits.

UNIT IV ARITHMETIC BUILDING BLOCKS 9

Data path circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Speed and Area Tradeoffs

UNIT V MEMORY ARCHITECTURES 6

Memory Architectures and Memory control circuits : Read-Only Memories, ROM cells, Read-write memories (RAM), dynamic memory design, 6 transistor SRAM cell, Sense amplifiers.

TOTAL : 45 PERIODS

COURSE OUTCOMES:

- To use mathematical methods and circuit analysis models in analysis of CMOS digital circuits
- To be able to create models of moderately sized static CMOS combinational circuits that realize specified digital functions and to optimize combinational circuit delay using RC delay models and logical effort
- To design sequential logic at the transistor level and Compare the tradeoffs of sequencing elements including flip-flops, transparent latches
- To learn design methodology of arithmetic building blocks
- To design functional units including ROM and SRAM

REFERENCES:

1. Jan Rabaey, Anantha Chandrakasan, B Nikolic, “ Digital Integrated Circuits: A Design Perspective”, Prentice Hall of India, 2nd Edition, Feb 2003,
2. N.Weste, K. Eshraghian, “ Principles of CMOS VLSI Design”, Addision Wesley, 2nd Edition, 1993
3. M J Smith, “Application Specific Integrated Circuits”, Addisson Wesley, 1997
4. Sung-Mo Kang & Yusuf Leblebici, “CMOS Digital Integrated Circuits Analysis and Design”, McGraw-Hill, 1998.

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		2	1		
CO2	3		2	1		
CO3	3		2	1		
CO4	3		3	2	1	1
CO5	3		3	2	1	1

AP5151 ANALOG INTEGRATED CIRCUIT DESIGN L T P C
3 0 0 3

OBJECTIVES:

- Analog circuits play a very crucial role in all electronic systems and due to continued miniaturization, many of the analog blocks are not getting realized in CMOS technology. The most important building blocks of all CMOS analog ICs will be the topic of study in this course.
- The basic principle of operation, the circuit choices and the tradeoffs involved in the MOS transistor level design common to all analog CMOS ICs will be discussed in this course.
- The specific design issues related to single and multistage voltage, current and differential amplifiers, their output and impedance issues, bandwidth, feedback and stability will be dealt with in detail.

UNIT I SINGLE STAGE AMPLIFIERS 9

Basic MOS physics and equivalent circuits and models, CS, CG and Source Follower differential with active load, Cascode and folded cascode configurations with active load, Design of differential and cascode amplifiers – to meet specified SR, noise, gain, BW, ICMR and power dissipation, voltage swing, High gain amplifier, structures.

UNIT II HIGH FREQUENCY AND NOISE OF CHARACTERISTICS AMPLIFIERS 9

Miller effect, association of poles with nodes, frequency response of CS, CG and source follower, cascode and differential pair stages, Statistical characteristics of noise, noise in single stage amplifiers, noise in differential amplifiers.

UNIT III FEEDBACK AND ONE STAGE OPERATIONAL AMPLIFIERS 9

Properties and types of negative feedback circuits, effect of loading in feedback networks, operational amplifier performance parameters, One-stage Op Amps, Two-stage Op Amps, Input range limitations, Gain boosting, slew rate, power supply rejection, noise in Op Amps.

UNIT IV STABILITY AND FREQUENCY COMPENSATION OF TWO STAGE AMPLIFIER 9

Analysis of two stage Op amp – two stage Op amp single stage CMOS Cs as second stage and using cascode second stage, multiple systems, Phase Margin, Frequency Compensation, and Compensation of two stage Op Amps, Slewing in two stage Op Amps, Other compensation techniques.

UNIT V BANDGAP REFERENCES 9

Current sinks and sources, Current mirrors, Wilson current source, Wildar current source, Cascode current source, Design of high swing cascode sink, current amplifiers, Supply independent biasing, temperature independent references, PTAT and CTAT current generation, Constant-Gm Biasing.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

CO1: Ability to design amplifiers to meet user specifications
CO2: Ability to analyse the frequency and noise performance of amplifiers
CO3: Ability to design and analyse feedback amplifiers and one stage op amps
CO4: Ability to design and analyse two stage op amps
CO5: Ability to design and use current mirrors and current sinks with MOS devices

REFERENCES:

1. Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, Tata McGraw Hill, 2001.
2. Willey M.C. Sansen, “Analog Design Essentials”, Springer, 2006.
3. Grebene, “Bipolar and MOS Analog Integrated circuit design”, John Wiley & sons,Inc.,2003.
4. Phillip E.Allen, DouglasR.Holberg, “CMOS Analog Circuit Design”, Oxford University Press, 2nd edition, 2002.
5. Recorded lecture available at http://www.ee.iitm.ac.in/~ani/ee5390/index.html
6. Jacob Baker “CMOS: Circuit Design, Layout, and Simulation, Third Edition”, Wiley IEEE Press, 3rd Edition, 2010

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2		3			
CO2	2		3		1	
CO3	2		3		1	
CO4	2		3		1	
CO5	2		3		1	

VL5151 ASIC DESIGN L T P C
3 0 0 3

OBJECTIVES:

- The course focuses on the semi-custom IC Design and introduces the principles of design logic cells, I/O cells and interconnect architecture, with equal importance given to FPGA and ASIC styles.
- The entire FPGA and ASIC design flow is dealt with from the circuit and layout design point of view.

UNIT I INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN 9

Types of ASICs - Design flow - CMOS transistors - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort.

UNIT II PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS 9

Anti fuse - static RAM - EPROM and EEPROM technology - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT III PROGRAMMABLE ASIC ARCHITECUTRE 9

Architecture and configuration of Artix / Cyclone and Kintex Ultra Scale / Stratix FPGAs – Micro-Blaze / Nios based embedded systems – Signal probing techniques.

UNIT IV LOGIC SYNTHESIS, PLACEMENT AND ROUTING 9

Logic synthesis - Floor Planning Goals and Objectives, Measurement of Delay in floor planning, Floor planning tools ,I/O and Power planning, Clock planning, Placement Algorithms. Routing: Global routing, Detailed routing,Special routing.

UNIT V SYSTEM-ON-CHIP DESIGN 9

SoC Design Flow, Platform-based and IP based SoC Designs, Basic Concepts of Bus-Based Communication Architectures, High performance filters using delta-sigma modulators.
Case Studies: Digital camera, SDRAM, High speed data standards.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

CO1: Ability to apply logical effort technique for predicting delay, delay minimization and FPGA architectures
CO2: Ability to design logic cells and I/O cells
CO3: Ability to analyze the various resources of recent FPGAs
CO4: Ability to use algorithms for floor planning and placement of cells and to apply routing algorithms for optimization of length and speed.
CO5: Ability to analyze high performance algorithms available for ASICs

REFERENCES:

1. M.J.S.Smith, " Application - Specific Integrated Circuits", Pearson, 2003.
2. Steve Kilts, “Advanced FPGA Design,” Wiley Inter-Science.
3. Roger Woods, John McAllister, Dr. Ying Yi, Gaye Lightbod, “FPGA-based Implementation of Signal Processing Systems”, Wiley, 2008.
4. Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and Information Processing ", Mc Graw Hill, 1994.
5. Douglas J. Smith, “HDL Chip Design”, Madison, AL, USA: Doone Publications, 1996.
6. Jose E. France, Yannis Tsividis, "Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing", Prentice Hall, 1994.
7. S.Pasricha and N.Dutt, “On-Chip Communication Architectures System on Chip Interconnect”, Elsveir, 2008.

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		2	1		
CO2	3		2	1		
CO3	3		2	1		
CO4	3		3	2	1	1
CO5	3		3	2	1	1

RM5151 RESEARCH METHODOLOGY AND IPR LT P C
2 0 0 2

OBJECTIVES:

To impart knowledge and skills required for research and IPR:

- Problem formulation, analysis and solutions.
- Technical paper writing / presentation without violating professional ethics
- Patent drafting and filing patents.

UNIT I RESEARCH PROBLEM FORMULATION 6

Meaning of research problem- Sources of research problem, criteria characteristics of a good research problem, errors in selecting a research problem, scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, necessary instrumentations

UNIT II LITERATURE REVIEW 6

Effective literature studies approaches, analysis, plagiarism, and research ethics.

UNIT III TECHNICALWRITING /PRESENTATION 6

Effective technical writing, how to write report, paper, developing a research proposal, format of research proposal, a presentation and assessment by a review committee.

UNIT IV INTRODUCTION TO INTELLECTUAL PROPERTY RIGHTS (IPR) 6

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT V INTELLECTUAL PROPERTY RIGHTS (IPR) 6

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications. New Developments in IPR: Administration of Patent System, IPR of Biological Systems, Computer Software etc.
Traditional knowledge Case Studies, IPR and IITs.

TOTAL: 30 PERIODS

COURSE OUTCOMES:

CO1: Ability to formulate research problem
CO2: Ability to carry out research analysis
CO3: Ability to follow research ethics
CO4: Ability to understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity
CO5: Ability to understand about IPR and filing patents in R & D.

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	✓	✓										
CO2	✓											
CO3	✓							✓				
CO4	✓				✓							
CO5	✓					✓						✓

REFERENCES:

1. Asimov, “Introduction to Design”, Prentice Hall, 1962.
2. Halbert, “Resisting Intellectual Property”, Taylor & Francis Ltd ,2007.
3. Mayall, “Industrial Design”, McGraw Hill, 1992.
4. Niebel, “Product Design”, McGraw Hill, 1974.
5. Ranjit Kumar,“Research Methodology: A Step by Step Guide for beginners” 2nd Edition, 2010.

VL5161 ANALOG AND DIGITAL CMOS VLSI DESIGN LABORATORY L T P C
0 0 4 2

OBJECTIVES:

- Students will carry out a detailed analog circuit design starting with transistor characterization and finally realizing an IA design.
- At various stages of design, a typical state of art CAD VLSI tool will be used in various phases of experiments designed to bring out the key aspects of each important module in the CAD tool including the simulation, layout, LVS and parasitic extracted simulation.

List of Experiments:

1. Extraction of process parameters of CMOS process transistors
   a. Plot I_D vs. V_{GS} at different drain voltages for NMOS, PMOS.
   b. Plot I_D vs. V_{GS} at particular drain voltage (low) for NMOS, PMOS and determine Vt.
   c. Plot log I_D vs. VGS at particular gate voltage (high) for NMOS, PMOS and determine I_{OFF} and sub-threshold slope.
   d. Plot I_D vs. V_{DS} at different gate voltages for NMOS, PMOS and determine Channel length modulation factor.
   e. Extract V_{th} of NMOS/PMOS transistors (short channel and long channel). Use V_{DS} of appropriate voltage To extract V_{th} use the following procedure.
      i. Plot g_m vs V_{GS} using SPICE and obtain peak g_m point.
      ii. Plot $y=I_D/(g_m)$ as a function of VGS using SPICE.
      iii. Use SPICE to plot tangent line passing through peak gm point in y (V_{GS}) plane and determine V_{th}.
   f. Plot I_D vs. V_{DS} at different drain voltages for NMOS, PMOS, plot DC load line and calculate gm, gds, gm/gds, and unity gain frequency. Tabulate result according to technologies and comment on it.
2. CMOS inverter design and performance analysis
   a. i. Plot VTC curve for CMOS inverter and thereon plot dV_{out} vs. dV_{in} and determine transition voltage and gain g. Calculate V_{IL}, V_{IH}, NM_H, NM_L for the inverter.
      ii. Plot VTC for CMOS inverter with varying V_{DD}.
      iii. Plot VTC for CMOS inverter with varying device ratio.
   b. Perform transient analysis of CMOS inverter with no load and with load and determine t_{pHL}, t_{pLH}, 20%-to-80% t_r and 80%-to-20% t_f.
   c. Perform AC analysis of CMOS inverter with fanout 0 and fanout 1.
3. Use spice to build a three stage and five stage ring oscillator circuit and compare its frequencies. Use FFT and verify the amplitude and frequency components in the spectrum.
4. Single stage amplifier design and performance analysis
   a. Draw small signal voltage gain of the minimum-size inverter in the technology chosen as a function of input DC voltage. Determine the small signal voltage gain at the switching point using spice and compare the values for two different process transistors.
   b. Consider a simple CS amplifier with active load, with NMOS transistor as driver and PMOS transistor as load.
      i. Establish a test bench to achieve $V_{DSQ}=V_{DD}/2$.
      ii. Calculate input bias voltage for a given bias current.
      iii. Use spice and obtain the bias current. Compare with the theoretical value
      iv. Determine small signal voltage gain, -3dB BW and GBW of the amplifier

using small signal analysis in spice, considering load capacitance.

v. Plot step response of the amplifier with a specific input pulse amplitude. Derive time constant of the output and compare it with the time constant resulted from -3dB BW.

vi. Use spice to determine input voltage range of the amplifier

5. Three OPAMP Instrumentation Amplifier.

Use proper values of resistors to get a three OPAMP INA with differential-mode voltage gain=10. Consider voltage gain=2 for the first stage and voltage gain=5 for the second stage.

i. Draw the schematic of op-amp macro model.

ii. Draw the schematic of INA.

iii. Obtain parameters of the op-amp macro model such that it meets a given specification for:

i. low-frequency voltage gain,
ii. unity gain BW (fu),
iii. input capacitance,
iv. output resistance,
v. CMRR

d. Draw schematic diagram of CMRR simulation setup.

e. Simulate CMRR of INA using AC analysis (it's expected to be around 6dB below CMRR of OPAMP).

f. Plot CMRR of the INA versus resistor mismatches (for resistors of second stage only) changing from -5% to +5% (use AC analysis). Generate a separate plot for mismatch in each resistor pair. Explain how CMRR of OPAMP changes with resistor mismatches.

g. Repeat (iii) to (vi) by considering CMRR of all OPAMPs with another low frequency gain setting.

6. Use Layout editor.

a. Draw layout of a minimum size inverter using transistor from CMOS process library. Use Metal 1 as interconnect line between inverters.

b. Run DRC, LVS and RC extraction. Make sure there is no DRC error.

c. Extract the netlist. Use extracted netlist and obtain t_{PHL} t_{PLH} for the inverter using Spice.

d. Use a specific interconnect length and connect and connect three inverters in a chain. Extract the new netlist and obtain t_{PHL} and t_{PLH} of the middle inverter.

e. Compare new values of delay times with corresponding values obtained in part ‘c’.

7. Design a differential amplifier with resistive load using transistors from CMOS process library that meets a given specification for the following parameter

a. low-frequency voltage gain,

b. unity gain BW (fu),

c. Power dissipation

i. Perform DC analysis and determine input common mode range and compare with the theoretical values.

ii. Perform time domain simulation and verify low frequency gain.

iii. Perform AC analysis and verify.

TOTAL:60 PERIODS

COURSE OUTCOMES:

CO1: Design digital and analog Circuit using CMOS given a design specification.

CO2: Design and carry out time domain and frequency domain simulations of simple analog building blocks, study the pole zero behaviors and compute the input/output impedances

CO3: Use EDA tools like Cadence, Mentor Graphics or other open source software tools like LTSpice

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	1	3	3	2	2
CO2	3	1	3	3	2	2
CO3	3	1	3	3	2	2

AP5261 PRINTED CIRCUIT BOARD DESIGN AND COMPONENT ASSEMBLING LABORATORY **L T P C 0 0 4 2**

OBJECTIVES

- To impart hands on experience in single, double and multi layer PCB design so that students would be able to design and to fabricate and develop electronic systems for various applications.

LIST OF EXPERIMENTS:

1. Introduction to PCB and EDA software tools.
2. To prepare design layout of PCBs using software tools.
3. To fabricate simple PCB by chemical and mechanical process and drilling of PCB.
4. To fabricate PCB using additive technology and testing of electronics circuit on PCB.
5. To perform Assembly Processes -Manual assembly processes,
6. To perform automated assembly processes (pick and place).
7. Identification of various types of Printed Circuit Boards (PCB) and soldering Techniques.
8. Convert the power supply circuit into PCB and simulate its 2D and 3D view.
9. Design and create single sided PCB Layout for Full wave rectifier circuit.
10. Design and create PCB Layout for DC Motor controller.
11. Design and create single sided PCB Layout for Flashing LEDs using 555 IC.
12. LED Scrolling Display Board using microcontroller
13. To perform continuity tester of PCB project.
14. To implement a Digital Counter To fabricate the PCB for the same.
15. To fabricate PCB dual power supply, analog design.
16. To fabricate PCB with Split power and ground planes.

TOTAL : 60 PERIODS

COURSE OUTCOMES:

CO1: Ability to use CAD software tools
CO2: Ability to design a schematic diagram
CO3: Ability to convert a schematic diagram to board/layout diagram
CO4: Implement routing in board/layout diagram
CO5: Ability to fabricate a PCB from board diagram
CO6: Ability to skillfully perform assembling and soldering of components

	PO1	PO2	PO3	PO4	PO5	PO6
CO1				3		
CO2		1	1	2		
CO3			3		1	
CO4				3	2	
CO5					1	
CO6			3			2

AP5152 EMBEDDED SYSTEM DESIGN **L T P C 3 0 0 3**

OBJECTIVES:

- To expose the students to the fundamentals of embedded system design.
- To enable the students to understand and use embedded computing platform.
- To introduce networking principles in embedded devices.
- To learn real time characteristics in embedded system design.
- To explore system design techniques.

UNIT I EMBEDDED PROCESSORS 9

Embedded Computers, Characteristics of Embedded Computing Applications, Challenges in Embedded Computing system design, Embedded system design process- Requirements, Specification, Architectural Design, Designing Hardware and Software Components, System Integration, Formalism for System Design- Structural Description, Behavioural Description, Design Example: Model Train Controller, ARM processor- processor and memory organization.

UNIT II EMBEDDED COMPUTING PLATFORM 9

Data operations, Flow of Control, SHARC processor- Memory organization, Data operations, Flow of Control, parallelism with instructions, CPU Bus configuration, ARM Bus, SHARC Bus, Memory devices, Input/output devices, Component interfacing, designing with microprocessor development and debugging, Design Example : Alarm Clock.

UNIT III NETWORKS 9

Distributed Embedded Architecture- Hardware and Software Architectures, Networks for embedded systems- I2C, CAN Bus, SHARC link supports, Ethernet, Myrinet, Internet, Network-Based design- Communication Analysis, system performance Analysis, Hardware platform design, Allocation and scheduling, Design Example: Elevator Controller.

UNIT IV REAL-TIME CHARACTERISTICS 9

Clock driven Approach, weighted round robin Approach, Priority driven Approach, Dynamic Versus Static systems, effective release times and deadlines, Optimality of the Earliest deadline first (EDF) algorithm, challenges in validating timing constraints in priority driven systems, Off-line Versus On-line scheduling.

UNIT V SYSTEM DESIGN TECHNIQUES 9

Design Methodologies, Requirement Analysis, Specification, System Analysis and Architecture Design, Quality Assurance, Design Example: Telephone PBX- System Architecture, Ink jet printer- Hardware Design and Software Design, Personal Digital Assistants, Set-top Boxes.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

CO1: To explore fundamentals of embedded system design.
CO2: To interpret and use embedded computing platform.
CO3: To apply networking principles in embedded devices.
CO4: To gain insight on the characteristics in embedded system design.
CO5: To select and design suitable embedded systems for real world applications.

REFERENCES:

1. Wayne Wolf, “Computers as Components: Principles of Embedded Computing System Design”, Morgan Kaufman Publishers, 3rd edition, 2012.
2. Jane.W.S. Liu, “Real-Time systems”, Pearson Education Asia, 2001.
3. C. M. Krishna and K. G. Shin, “Real-Time Systems” , McGraw-Hill, 1997 .
4. Frank Vahid and Tony Givargis, “Embedded System Design: A Unified Hardware/Software Introduction”, John Wiley & Sons, 2002.

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1					
CO2		2			1	
CO3			1	2		
CO4					3	1
CO5					2	3

VL5251 **LOW POWER VLSI DESIGN** **L T P C**
3 0 0 3

OBJECTIVES:

- Identify sources of power in an IC.
- Identify the power reduction techniques based on technology independent and technology dependent methods
- Identify suitable techniques to reduce the power dissipation.
- Estimate Power dissipation of various MOS logic circuits.
- Develop algorithms for low power dissipation.

UNIT I POWER DISSIPATION IN CMOS 9

Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOS FET devices – Basic principle of low power design.

UNIT II POWER OPTIMIZATION 9

Logic level power optimization – Circuit level low power design – Gate level low power design – Architecture level low power design – VLSI subsystem design of adders, multipliers, PLL, low power design.

UNIT III DESIGN OF LOW POWER CMOS CIRCUITS 9

Computer arithmetic techniques for low power system – reducing power consumption in combinational logic, sequential logic, memories – low power clock – Advanced techniques – Special techniques, Adiabatic techniques – Physical design, Floor planning, placement and routing.

UNIT IV POWER ESTIMATION 9

Power Estimation techniques, circuit level, gate level, architecture level, behavioral level, – logic power estimation – Simulation power analysis –Probabilistic power analysis.

UNIT V SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER 9

Synthesis for low power – Behavioral level transform –Algorithms for low power – software design for low power.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

CO1: Ability to find the power dissipation of MOS circuits
CO2: Design and analyse various MOS logic circuits
CO3: Apply low power techniques for low power dissipation
CO4: Able to estimate the power dissipation of ICs
CO5: Ability to develop algorithm to reduce power dissipation by software.

REFERENCES:

1. Kaushik Roy and S.C.Prasad, “Low power CMOS VLSI circuit design”, Wiley, 2000.
2. J.B.Kulo and J.H Lou, “Low voltage CMOS VLSI Circuits”, Wiley 1999.
3. A.P.Chandrasekaran and R.W.Broadersen, “Low power digital CMOS design”, Kluwer,1995.
4. Gary Yeap, “Practical low power digital VLSI design”, Kluwer, 1998.
5. Abdelatif Belaouar, Mohamed.I.Elmasry, “Low power digital VLSI design”, Kluwer, 1995.
6. James B.Kulo, Shih-Chia Lin, “Low voltage SOI CMOS VLSI devices and Circuits”, John Wiley and sons, inc. 2001.
7. J.Rabaey, “Low Power Design Essentials (Integrated Circuits and Systems)”, Springer, 2009

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1					
CO2		2			1	
CO3			1	2		
CO4					3	1
CO5					2	3

AP5153 STATISTICAL SIGNAL PROCESSING L T P C
3 0 0 3

OBJECTIVES:

- To introduce the basics of random signal processing
- To learn the concept of estimation and prediction theory
- To know about adaptive filtering and its applications

UNIT I INTRODUCTION TO RANDOM SIGNAL PROCESSING 9

Discrete Random Processes- Ensemble Averages, Stationary processes, Bias and Estimation, Autocovariance, Autocorrelation, Parseval‟s theorem, Wiener-Khintchine relation, White noise, Power Spectral Density, Spectral factorization, Filtering Random Processes.

UNIT II SIGNAL MODELING 9

ARMA (p,q) , AR (p), MA (q) models, Forward Linear Prediction, Backward Linear Prediction : – Yule-Walker Method, Solution to Prony's normal equation, Levinson Durbin Algorithm.

UNIT III SPECTRAL ESTIMATION 9

Estimation of spectra from finite duration signals, Nonparametric methods - Periodogram, Modified periodogram, Bartlett, Welch and Blackman-Tukey methods, Parametric method, AR (p) spectral estimation and detection of Harmonic signals.

UNIT IV LINEAR ESTIMATION 9

Linear Minimum Mean-Square Error (LMMSE) Filtering: Wiener Hopf Equation, FIR Wiener filter, Noise Cancellation, Causal IIR Wiener filter, Noncausal IIR Wiener filter.

UNIT V ADAPTIVE FILTERS 9

FIR adaptive filters – adaptive filter based on steepest descent method- Widrow-Hopf LMS algorithm, Normalized LMS algorithm, Adaptive channel equalization, Adaptive echo cancellation, Adaptive noise cancellation, RLS adaptive algorithm.

TOTAL : 45 PERIODS

COURSE OUTCOMES:

CO1: Analyze discrete time random processes
CO2: Obtain models for prediction and Estimation
CO3:Analyze non-parametric methods and parametric methods for spectral estimation
CO4: Design different MMSE filters
CO5: Design adaptive filters for different applications

REFERENCES:

1. Monson H. Hayes, “Statistical Digital Signal Processing and Modeling”, John Wiley and Sons, Inc, Singapore, 2002.
2. Dimitris G. Manolakis and Vinay K .Ingle ,“Applied Digital Signal Processing”, Cambridge University Press, 2011.
3. Fundamentals of Statistical Signal Processing: Estimation Theory(Vol 1), Detection Theory (Vol 2), .M. Kay's, Prentical Hall Signal Processing Series, 1993.
4. Linear Estimation, Kailath, Sayed and Hassibi, Prentical Hall Information and Sciences Series, 1st Edition, 2000.

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		2	1		
CO2	3		2	1		
CO3	3		3	1		
CO4	3		3	2	1	1
CO5	3		3	2	1	1

AP5161 EMBEDDED SYSTEMS AND ROBOTICS LABORATORY L T P C
0 0 4 2

OBJECTIVES:

- To introduce microcontroller based system design concept.
- To learn concept on real time operating systems..
- To make learn EDA tools, sensors, high power devices and motors.
- To work with different Robots and its operating systems.

EMBEDDED SYSTEMS LAB EXPERIMENTS:

1. Microcontroller based system design of interfacing with RTC, LCD and I2C EPROM.
2. Design of microcontroller based RC5 remote control decoder.
3. Microcontroller based system design of Switching of high power device with SCR, MOSFET and Relay.
4. Microcontroller based system design with Touch screen interfacing.
5. Sensors and interfacing of ultrasound sensors, PIR, temperature and RFID with Microcontroller based system.
6. Microcontroller based system design with Matrix keyboard and LED interfacing.
7. Microcontroller based system design with Motor interfacing-DC, servo and stepper.
8. Design and implementation of different real time scheduling algorithms for embedded applications. RTOS- simple task creation, Round Robin Scheduling and Semaphores.

ROBOTICS LAB EXPERIMENTS:

1. Design and implementation of Line following Robot.
2. Design and implementation of Obstacle avoidance and navigation Robot.
3. Design and implementation of Robotic Arm manipulation with 6 DOF.
4. Design and implementation of Pick and Place robot.
5. Design and implementation of Colour guided material handling Robot.

6. Design and implementation of Self balancing robot.
7. Robot operating System (ROS) for Robot.

COURSE OUTCOMES:

CO1: Ability to design and develop microcontroller based systems.
CO2: Validate the design in microcontroller starting from assembler to compiler.
CO3: Ability to use EDA tools, sensors, high power devices and motors.
CO4: Ability to design and develop different real-time scheduling algorithms.
CO5: Ability to work with different Robot operating systems.

TOTAL: 60 PERIODS

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1				2	
CO2			3			
CO3			2	2	1	
CO4			1	1		
CO5				3	1	1

VL5261 SIGNAL PROCESSING AND RTL SYNTHESIS LABORATORY L T P C
0 0 4 2

OBJECTIVES:

- FPGAs are important platform used throughout the industry both in their own right in building complete systems. They are also used as validation/verification platforms prior to undertaking cost and time intensive design and fabrication of custom VLSI designs. Starting from high level design entry in the form VHDL/Verilog codes, the students will be carrying out complete hardware level FPGA validation of important digital algorithms.
- Understanding signal processing play a key role in the design and testing of circuit block in ICs. The experiments are structured to give an exposure to the design of basic signal processing modules and its realization in FPGA

LIST OF EXPERIMENTS:

1) HDL realization and timing analysis of
   i. Combinational circuits namely 8:1 Mux/Demux, Full Adder, 8-bit Magnitude comparator, Encoder/decoder, Priority encoder.
   ii. Sequential circuits namely D-FF, 4-bit Shift registers (SISO, SIPO, PISO, bidirectional), 3-bit Synchronous Counters.
2) FPGA implementation of PCI Bus & arbiter.
3) Realization of UART/ USART implementation in HDL and design validation using test vector generation.
4) FPGA realization of single port SRAM and capturing the signal in DSO.
5) Back annotation and timing analysis of Arithmetic circuits like serial adder/ subtractor, parallel adder/subtractor, serial/parallel multiplier.
6) Realization of Discrete Fourier transform/Fast Fourier Transform algorithm in HDL and observing the spectrum in simulation.
7) Implement different power spectrum
8) Design and implement FIR and IIR Weiner filters for smoothing and prediction
9) Design and implement adaptive filters

10) Perform image enhancement operations (spatial & transform domain analysis)
11) Perform morphological image analysis
12) Implement image segmentation algorithms

TOTAL : 60 PERIODS

COURSE OUTCOMES:

CO1: Identify, formulate, solve and implement problems in signal processing, communication systems etc using RTL design tools.
CO2: Validate the design in FPGA starting from design entry to back annotation.
CO3: Use EDA tools like Cadence/Mentor Graphics/ Xilinx/Quartus.
CO4: Implement image processing algorithms using MATLAB and HDL
CO5: Implement image processing algorithms using MATLAB and HDL

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1	1	3	3	2	
CO2	1	1	3	3	2	
CO3	1	1	3	3	2	
CO4	1	1	3	2	2	
CO5	1	1	3	2	2	

AP5078 WIRELESS SENSOR NETWORKS L T P C
3 0 0 3

OBJECTIVES:

- To enable the student to understand the role of sensors and the networking of sensed data for different applications.
- To expose the students to the sensor node essentials and the architectural details, the medium access and routing issues and the energy constrained operational scenario.
- To enable the student to understand the challenges in synchronization and localization of sensor nodes, topology management for effective and sustained communication, data management and security aspects

UNIT I OVERVIEW OF WIRELESS SENSOR NETWORKS 9

Challenges for Wireless Sensor Networks-Characteristics requirements-required mechanisms, Difference between mobile ad-hoc and sensor networks, Applications of sensor networks- case study, Enabling Technologies for Wireless Sensor Networks.

UNIT II ARCHITECTURES 9

Single-Node Architecture - Hardware Components, Energy Consumption of Sensor Nodes , Operating Systems and Execution Environments, Network Architecture - Sensor Network Scenarios, Optimization Goals and Figures of Merit, Gateway Concepts. Physical Layer and Transceiver Design Considerations

UNIT III MAC AND ROUTING 9

MAC Protocols for Wireless Sensor Networks, IEEE 802.15.4, Zigbee, Low Duty Cycle Protocols And Wakeup Concepts - S-MAC , The Mediation Device Protocol, Wakeup Radio Concepts, Address and Name Management, Assignment of MAC Addresses, Routing Protocols- Energy- Efficient Routing, Geographic Routing.

UNIT IV INFRASTRUCTURE ESTABLISHMENT 9

Topology Control, Clustering, Time Synchronization, Localization and Positioning, Sensor Tasking and Control.

UNIT V DATA MANAGEMENT AND SECURITY 9

Data management in WSN, Storage and indexing in sensor networks, Query processing in sensor, Data aggregation, Directed diffusion, Tiny aggregation, greedy aggregation, security in WSN.

TOTAL : 45 PERIODS

COURSE OUTCOMES:

CO1: Ability to design implement simple wireless network concepts
CO2: Ability to design, analyze implement different network architectures
CO3: Ability to implement MAC layer and routing protocols
CO4: Ability to deal with timing and control issues in wireless sensor networks
CO5: Ability to analyze and design secured wireless sensor networks

REFERENCES

1. Ian F. Akyildiz, Mehmet Can Vuran, “Wireless Sensor Networks”, John Wiley, 2010
2. Yingshu Li, My T. Thai,Weili Wu, “Wireless Sensor Networks and Applications”, Springer, 2008.
3. Holger Karl & Andreas Willig, "Protocols And Architectures for Wireless Sensor Networks" , John Wiley, 2005.
4. Feng Zhao & Leonidas J. Guibas, “Wireless Sensor Networks- An Information Processing Approach", Elsevier, 2007.
5. Kazem Sohraby, Daniel Minoli, & Taieb Znati, “Wireless Sensor Networks-s Technology, Protocols, And Applications”, John Wiley, 2007.
6. Anna Hac, “Wireless Sensor Network Designs”, John Wiley, 2003.
7. Bhaskar Krishnamachari, “Networking Wireless Sensors”, Cambridge Press,2005.
8. Mohammad Ilyas And Imad Mahgaob, “Handbook Of Sensor Networks: Compact Wireless And Wired Sensing Systems”, CRC Press,2005.
9. Wayne Tomasi, “Introduction To Data Communication And Networkingǁ, Pearson Education”, 2007.

COs	Programme Outcomes					
	PO1	PO2	PO3	PO4	PO5	PO6
1			1	2		
2			2	2		
3	1		3	3	1	1
4	1		2	2		
5	1		2	3	1	1

AP5074 PCB DESIGN AND FABRICATION L T P C
3 0 0 3

OBJECTIVES:

- To expose the students to the basics of PCB design
- To lead the new users of the software through a very simple design
- To address the mechanical aspect of PCB design and to aid in understanding the design issues, manufacturing processes.
- To address the electrical aspect of PCB design
- To expose the students to the state of art technology in PCB design and manufacturing

UNIT I BASICS OF PCB DESIGN, TOOLS & INDUSTRY STANDARDS 9

Printed Circuit Board Fabrication- PCB cores and layer stack-up. PCB fabrication process- Photolithography and chemical etching, Mechanical Layer registration. Function of the Layout in the PCB Design Process. Design Files Created by Layout - Layout format files, Postprocess (Gerber) files, PCB assembly layers and files. Introduction to the Standards Organizations, Classes and Types of PCBs, Introduction to Standard Fabrication Allowances, PCB Dimensions and Tolerances, Copper Trace and Etching Tolerances, Standard Hole Dimensions, Soldermask Tolerance.

UNIT II PCB DESIGN FLOW USING CAD TOOL 9

Overview of Computer-Aided Design. Project structures and the layout toolset- Project Setup and Schematic Entry Details, the Layout Environment and Tool Set. Creating a Circuit Design with Capture-Starting a new project placing parts, Wiring (connecting) the parts, creating the Layout netlist in Capture. Designing the PCB with Layout- Starting Layout and importing the netlist, Performing a design rule check, Making a board outline, Placing the parts, Auto routing the board Manual routing, Cleanup Locking traces, Post processing the board design for manufacturing. Setting up a user account, Submitting Gerber files and requesting a quote, Annotating the layer types and stack-up, Receipt inspection and testing, Nonstandard Gerber files.

UNIT III DESIGN FOR MANUFACTURING 9

PCB Assembly and Soldering Processes- Component Placement and Orientation Guide, Component Spacing for Through-hole Devices. Component Spacing for Surface Mounted Devices SMDs, Mixed THD and SMD Spacing Requirements. Footprint and Padstack Design for PCB Manufacturability- Land Patterns for Surface-Mounted Devices- Land Patterns for Through-hole Devices, Padstack design, Hole-to-lead ratio, PTH land dimension (annular ring width), Clearance between plane layers and PTHs Soldermask and solder paste dimensions.

UNIT IV PCB DESIGN FOR SIGNAL INTEGRITY 9

Circuit Design Issues Not Related to PCB Layout, Issues Related to PCB Layout, Ground Planes and Ground Bounce, PCB Electrical Characteristics, PCB Routing Topics, Making and editing capture parts, The Capture Part Libraries, Types of Packaging, Pins, Part Editing Tools, Constructing Capture Parts, making and editing layout footprints.

UNIT V EMERGING ADDITIVE PROCESSES FOR PCB MANUFACTURING 9

Fundamentals of additive manufacturing, classification, advantages and standards on Additive manufacturing. Stereo lithography (SL), Stereo lithography (SL), Fused Deposition Modelling (FDM), Three Dimensional Printing (3DP), Materials, Applications. Voltera-V-one PCB double side Printer, Bot Factory- SV2-multi layer PCB printer, LPKF circuit board plotter and LDS Prototyping.

TOTAL : 45 PERIODS

COURSE OUTCOMES

CO1: To understand the basics, industry standards organizations related to the design and fabrication of PCBs.
CO2: Leads new users of the software through a very simple design
CO3: To know and guide in designing plated through-holes, surface-mount lands, and Layout footprints in general.
CO4: To know to construct Capture parts using the Capture Library Manager and Part Editor and the PSpice Model Editor.
CO5: To understand and to fabricate PCBs

REFERENCES:

1. Kraig Mitzner, Complete PCB Design Using OrCad Capture and Layout, Newness, 1st Edition, 2009.
2. Simon Monk, "Make Your Own PCBs with EAGLE: From Schematic Designs to Finished Boards", McGraw-Hill Education TAB, 2nd Edition, 2017.
3. Douglas Brooks, "Signal Integrity Issues and Printed Circuit Board Design", Prentice Hall PTR, 2003.
4. Lee W. Ritchey , John Zasio, Kella J. Knack, " Right the First Time: a Practical Handbook on High Speed Pcb and System Design", Speeding Edge , 2003.

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1	1				
CO2		1	3			
CO3		1	2			
CO4		1	2	3		
CO5			1	3	2	3

AP5071 ADVANCED MICROPROCESSORS & MICROCONTROLLERS L T P C
3 0 0 3

OBJECTIVES:

- To expose the students to the fundamentals of microprocessor architecture.
- To explore the high performance features in CISC architecture
- To familiarize the high performance features in RISC architecture
- To introduce the basic features in Motorola microcontrollers.
- To enable the students to understand PIC Microcontroller

UNIT I MICROPROCESSOR ARCHITECTURE 9

Instruction Set – Data formats –Addressing modes – Memory hierarchy –register file – Cache – Virtual memory and paging – Segmentation- pipelining –the instruction pipeline – pipeline hazards – instruction level parallelism – reduced instruction set –Computer principles – RISC versus CISC.

UNIT II HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM 9

CPU Architecture- Bus Operations – Pipelining – Brach predication – floating point unit- Operating Modes –Paging – Multitasking – Exception and Interrupts – Instruction set – addressing modes – Programming the Pentium processor.

UNIT III HIGH PERFORMANCE RISC ARCHITECTURE – ARM 9

Organization of CPU – Bus architecture –Memory management unit - ARM instruction set- Thumb Instruction set- addressing modes – Programming the ARM processor.

UNIT IV MSP430 16 - BIT MICROCONTROLLER 9

The MSP430 Architecture- CPU Registers - Instruction Set, On-Chip Peripherals - MSP430 - Development Tools, ADC - PWM - UART - Timer Interrupts - System design using MSP430Microcontroller.

UNIT V PIC MICROCONTROLLER 9

CPU Architecture – Instruction set – interrupts- Timers- I2C Interfacing –UART- A/D Converter –PWM and introduction to C-Compilers.

TOTAL:45 PERIODS

COURSE OUTCOMES:

CO1: To understand the fundamentals of microprocessor architecture.
CO2: To know and appreciate the high performance features in CISC architecture.
CO3: To know and appreciate the high performance features in RISC architecture.
CO4: To perceive the basic features in Motorola microcontrollers.
CO5: To interpret and understand PIC Microcontroller.

REFERENCES:

1. Daniel Tabak , „" Advanced Microprocessors" McGraw Hill.Inc., 1995
2. James L. Antonakos , " The Pentium Microprocessor", Pearson Education , 1997.
3. Steve Furber , " ARM System –On –Chip architecture", Addision Wesley , 2000.
4. Gene .H.Miller ." Micro Computer Engineering ", Pearson Education , 2003.
5. John .B.Peatman , " Design with PIC Microcontroller" , Prentice hall, 1997.
6. John H.Davis , "MSP 430 Micro controller basics", Eelsevier, 2008.
7. James L.Antonakos, "An Introduction to the Intel family of Microprocessors", Pearson Education 1999.
8. Barry.B.Breg, "The Intel Microprocessors Architecture , Programming and Interfacing " , PHI,2002.
9. Valvano "Embedded Microcomputer Systems" Thomson Asia PVT LTD first reprint 2001. Readings: Web links -- www.ocw.mit.edu, www.arm.com

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1		1			
CO2	1			3	1	1
CO3	1			3	1	1
CO4	1		1	3	2	1
CO5	1		1	3	2	1

AP5072 ELECTRONICS FOR SOLAR POWER L T P C
3 0 0 3

OBJECTIVES

- Study the behavior of photovoltaic solar energy systems, focusing on the behavior of "stand-alone" systems.
- Do a first order, conceptual design of a stand-alone system for a location anywhere in India
- Introduce the hardware elements and their behavior.
- Select battery for a PV system and battery sizing
- Simulate standalone and grid tied PV system

UNIT I INTRODUCTION TO SOLAR POWER 9

Semiconductor – properties - energy levels - basic equations of semiconductor devices physics - Basic characteristics of sunlight - Solar angles - day length - angle of incidence on tilted surface – Sun path diagrams – Equivalent circuit of PV cell, PV cell characteristics (VI curve, PV curve) - Maximum power point, Vmp, I_{MP}, Voc, I_{SC} – types of PV cell - Block diagram of solar photo voltaic system, PV array sizing.

UNIT II DC-DC CONVERTER 9

Principles of step-down and step-up converters – Analysis and design issues of buck, boost, buckboost and Cuk converters – time ratio and current limit control – Full bridge converter – Resonant and quasi – resonant converters.

UNIT III MAXIMUM POWER POINT TRACKING 9

Direct Energy transmission, Impedance Matching, Maximum Power PointTracking (MPPT) - Function of MPPT, P&O method, INC Method, Fractional Open circuit voltage method, Fractional short circuit current method, parasitic capacitance and other MPPT techniques, Development of hardware, algorithms using processors for Standalone and Grid tied systems.

UNIT IV BATTERY 9

Types of Battery, Battery Capacity – Units of Battery Capacity-impact of charging and discharging rate on battery capacity-Columbic efficiency-Voltage Efficiency, Charging – Charge Efficiency, Charging methods, State of Charge, Charging Rates, Discharging - Depth of discharge-Discharge Methods, Circuits for Battery Management System (BMS), selection of Battery and sizing.

UNIT V SIMULATION OF PV MODULE & CONVERTERS 9

Simulation of PV module - VI Plot, PV Plot, finding V_{MP}, I_{MP}, Voc, Isc of PV module, Simulation of DC to DC converter -buck, boost, buck-boost and Cuk converters, standalone and grid tied photo voltaic system.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

CO1: Ability to collect solar power characteristics at a given location
CO2: Ability to design and realize dc-dc converters for solar power utilization
CO3: Ability to design algorithms for improving solar power utilization
CO4: Ability to deal with battery issues and selection
CO5: Ability to design and simulate PV systems to validate its performance.

REFERENCES:

1. Chetan Singh Solanki, “Solar Photovoltaic: Fundamentals, Technologies and Applications”, PHI Ltd., 2013
2. Tommarkvart, Luis castaner, “Solar cells; materials, manufacture and operation”, Elsevier, 2005.
3. G.D .Rai, “Solar energy utilization “, Khanna publishes, 1993
4. Ned Mohan, Undeland and Robbin, “Power Electronics: converters, Application and Design”, John Wiley and sons.Inc, Newyork, 1995.

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	2	3	1	2	3
CO2	3	3	3	3	2	3
CO3	1	2	2	3	3	3
CO4	1	2	2	1	3	3
CO5	3	2	2	2	3	3

AP5076 ROBOTICS AND INTELLIGENT SYSTEMS L T P C
3 0 0 3

OBJECTIVES:

- To Teach the basic concepts in robotics.
- To expose the various design aspects in robot grippers.
- To make learn various drives and control systems.
- To impart knowledge on machine vision systems.
- To apply robot based concepts for automation

UNIT I INTRODUCTION: 9

Basic Concepts such as Definition, three laws, DOF, Misunderstood devices etc., Elements of Robotic Systems i.e. Robot anatomy, Classification, Associated parameters i.e. resolution, accuracy, repeatability, dexterity, compliance, RCC device, etc. Automation-Concept, Need, Automation in Production System, Principles and Strategies of Automation, Basic Elements of an Automated System, Advanced Automation Functions, Levels of Automations, introduction to automation productivity.

UNIT II ROBOT GRIPPERS: 9

Types of Grippers, Design aspect for gripper, Force analysis for various basic gripper system. Sensors for Robots:- Characteristics of sensing devices, Selections of sensors, Classification and applications of sensors. Types of Sensors, Need for sensors and vision system in the working and control of a robot.

UNIT III DRIVES AND CONTROL SYSTEMS: 9

Types of Drives, Actuators and its selection while designing a robot system. Types of transmission systems, Control Systems -Types of Controllers, Introduction to closed loop control .Control Technologies in Automation:- Industrial Control Systems, Process Industries Verses Discrete-Manufacturing Industries, Continuous Verses Discrete Control, Computer Process and its Forms. Control System Components such as Sensors, Actuators and others.

UNIT IV MACHINE VISION SYSTEM 9

Vision System Devices, Robot Programming:- Methods of robot programming, lead through programming, motion interpolation, branching capabilities, WAIT, SIGNAL and DELAY commands, subroutines, Programming Languages: Introduction to various types such as RAIL and VAL II etc, Features of type and development of languages for recent robot systems.

UNIT V MODELING AND SIMULATION FOR MANUFACTURING PLANT AUTOMATION 9

Introduction, need for system Modeling, Building Mathematical Model of a manufacturing Plant, Modern Tools- Artificial neural networks in manufacturing automation, AI in manufacturing, Fuzzy decision and control, robots and application of robots for automation. Artificial Intelligence:- Introduction to Artificial Intelligence, AI techniques, Need and application of AI. Other Topics in Robotics:- Socio-Economic aspect of robotisation. Economical aspects for robot design, Safety for robot and associated mass, New Trends & recent updates in robotics.

TOTAL:45 PERIODS

COURSE OUTCOMES:

- Ability to implement simple concepts associated with Robotics and Automation
- Ability to use various Robotic sub-systems
- Ability to use kinematics and dynamics to design exact working pattern of robots
- Ability to implement computer vison algorithms for robots
- Be aware of the associated recent updates in Robotics

REFERENCES:

1. John J. Craig, "Introduction to Robotics (Mechanics and Control)", Addison-Wesley, 2nd Edition, 2004
2. Mikell P. Groover et. Al., "Industrial Robotics: Technology, Programming and Applications, McGraw – Hill International", 1986.
3. Shimon Y. Nof , "Handbook of Industrial Robotics" , John Wiley Co, 2001.
4. Automation, "Production Systems and Computer Integrated Manufacturing", M.P. Groover, Pearson Education.
5. W.P. David, "Industrial Automation", John Wiley and Sons.
6. Richard D. Klafter , Thomas A. Chemielewski, Michael Negin, "Robotic Engineering : An Integrated Approach" , Prentice Hall India, 2002.
7. R.C. Dorf, "Handbook of design, manufacturing & Automation", John Wiley and Sons.

AP5075 RF SYSTEM DESIGN L T P C
3 0 0 3

OBJECTIVES:

- The students will learn various design steps starting from system specifications to hardware/software implementation and will experience process optimization while considering various design decisions.
- Students will gain design experience with project/case studies using contemporary high-level methods and tools.

UNIT I CMOS PHYSICS, TRANSCEIVER SPECIFICATIONS AND ARCHITECTURES 9

Introduction to MOSFET Physics, Noise: Thermal, shot, flicker, popcorn noise, Two port Noise theory, Noise Figure, THD, IP2, IP3, Sensitivity, SFDR, Phase noise - Specification distribution over a communication link, Homodyne Receiver, Heterodyne Receiver, Image reject, Low IF Receiver Architectures Direct upconversion Transmitter, Two step upconversion Transmitter.

UNIT II IMPEDANCE MATCHING AND AMPLIFIERS 9

S-parameters with Smith chart, Passive IC components, Impedance matching networks, Common Gate, Common Source Amplifiers, OC Time constants in bandwidth estimation and enhancement, High frequency amplifier design, Power match and Noise match, Single ended and Differential LNAs, Terminated with Resistors and Source Degeneration LNAs.

UNIT III FEEDBACK SYSTEMS AND POWER AMPLIFIERS 9

Stability of feedback systems: Gain and phase margin, Root-locus techniques, Time and Frequency domain considerations, Compensation, General model – Class A, AB, B, C, D, E and F amplifiers, Power amplifier Linearisation Techniques, Efficiency boosting techniques, ACPR metric, Design considerations

UNIT IV MIXERS AND OSCILLATORS 9

Mixer characteristics, Non-linear based mixers, Quadratic mixers, Multiplier based mixers, Single balanced and double balanced mixers, subsampling mixers, Oscillators describing Functions, Colpitts oscillators Resonators, Tuned Oscillators, Negative resistance oscillators, Phase noise.

UNIT V PLL AND FREQUENCY SYNTHESIZERS 9

Linearised Model, Noise properties, Phase detectors, Loop filters and Charge pumps, Integer-N frequency synthesizers, Direct Digital Frequency synthesizers.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

CO1: Ability to collect user specifications for RF systems
CO2: Ability to analyze and design RF amplifiers
CO3: Ability to analyze and design RF power amplifiers
CO4: Ability to analyze and design RF mixers and oscillators
CO5: Ability to design PLL for RF applications

REFERENCES:

1. T.Lee, “Design of CMOS RF Integrated Circuits”, Cambridge, 2004.
2. B.Razavi, “RF Microelectronics”, Pearson Education, 1997.
3. Jan Crols, Michiel Steyaert, “CMOS Wireless Transceiver Design”, Kluwer Academic Publishers, 1997.
4. B.Razavi, “Design of Analog CMOS Integrated Circuits”, McGraw Hill, 2001
5. Recorded lectures and notes available at . http://www.ee.iitm.ac.in/~ani/ee6240/

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		3	1	2	2
CO2	3		3	1	2	2
CO3	3		3	1	2	2
CO4	3		3	1	2	2
CO5	3		3	1	2	2

AP5077 SIGNAL INTEGRITY FOR HIGH SPEED DESIGN L T P C
3 0 0 3

OBJECTIVES:

- To identify sources affecting the speed of digital circuits.
- To introduce methods to improve the signal transmission characteristics

UNIT I SIGNAL PROPAGATION ON TRANSMISSION LINES 9

Transmission line equations, wave solution, wave *vs*. circuits, initial wave, delay time, Characteristic impedance , wave propagation, reflection, and bounce diagrams Reactive terminations – L, C , static field maps of micro strip and strip line cross-sections, per unit length parameters, PCB layer stackups and layer/Cu thicknesses, cross-sectional analysis tools, Zo and Td equations for microstrip and stripline Reflection and terminations for logic gates, fan-out, logic switching , input impedance into a transmission-line section, reflection coefficient, skin-effect, dispersion.

UNIT II MULTI-CONDUCTOR TRANSMISSION LINES AND CROSS-TALK 9

Multi-conductor transmission-lines, coupling physics, per unit length parameters ,Near and far-end cross-talk, minimizing cross-talk (stripline and microstrip) Differential signalling, termination, balanced circuits ,S-parameters, Lossy and Lossless models.

UNIT III NON-IDEAL EFFECTS 9

Non-ideal signal return paths – gaps, BGA fields, via transitions , Parasitic inductance and capacitance , Transmission line losses – Rs, tanδ , routing parasitic, Common-mode current, differential-mode current , Connectors.

UNIT IV POWER CONSIDERATIONS AND SYSTEM DESIGN 9

SSN/SSO , DC power bus design , layer stack up, SMT decoupling ,, Logic families, power consumption, and system power delivery , Logic families and speed Package types and parasitic ,SPICE, IBIS models ,Bit streams, PRBS and filtering functions of link-path components , Eye diagrams , jitter , inter-symbol interference Bit-error rate ,Timing analysis.

UNIT V CLOCK DISTRIBUTION AND CLOCK OSCILLATORS 9

Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, canceling parasitic capacitance, Clock jitter.

TOTAL : 45 PERIODS

COURSE OUTCOMES:

CO1:Ability to identify sources affecting the speed of digital circuits.
CO2;Ablility to identify methods to improve the signal transmission characteristics

REFERENCES

1. H. W. Johnson and M. Graham, High-Speed Digital Design: A Handbook of Black Magic, Prentice Hall, 1993.
2. Douglas Brooks, Signal Integrity Issues and Printed Circuit Board Design, Prentice Hall PTR , 2003.
3. S. Hall, G. Hall, and J. McCall, High-Speed Digital System Design: A Handboo of Interconnect Theory and Design Practices, Wiley-Interscience, 2000.
4. Eric Bogatin , Signal Integrity – Simplified , Prentice Hall PTR, 2003.

TOOLS REQUIRED

1. SPICE, source - http://www-cad.eecs.berkeley.edu/Software/software.html
2. HSPICE from synopsis, www.synopsys.com/products/ mixedsignal/hspice/hspice.html
3. SPECCTRAQUEST from Cadence, http://www.specctraquest.com

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2		3			1
CO2	2		3		1	
CO3	2		3		1	
CO4	2		3		1	
CO5	2		3		1	

AP5073 EMI AND EMC IN SYSTEM DESIGN L T P C
3 0 0 3

OBJECTIVES:

- To understand the concepts related to Electromagnetic interference in PCBs.
- To provide solutions for minimizing EMI in PCBs .
- To learn various EMI coupling principles.
- To indulge knowledge on EMI control techniques and design procedures to make EMI compatible PCBs
- To learn electromagnetic compatibility issues with regard to the design of PCBS
- To learn, EMI standards and measurements in the design of PCBs

UNIT I EMI/EMC CONCEPTS 9

EMI-EMC definitions and Units of parameters; Sources and victim of EMI; Conducted and Radiated EMI Emission and Susceptibility; Transient EMI, ESD; Radiation Hazards.

UNIT II EMI COUPLING PRINCIPLES 9

Conducted, radiated and transient coupling; Common ground impedance coupling; Common mode and ground loop coupling; Differential mode coupling; Near field cable to cable coupling, cross talk ; Field to cable coupling ; Power mains and Power supply coupling.

UNIT III EMI CONTROL TECHNIQUES 9

Shielding, Filtering, Grounding, Bonding, Isolation transformer, Transient suppressors, Cable routing, Signal control.

UNIT IV EMC DESIGN OF PCBS 9

Component selection and mounting; PCB trace impedance; Routing; Cross talk control; Power distribution decoupling; Zoning; Grounding; VIAs connection; Terminations

UNIT V EMI MEASUREMENTS AND STANDARDS 9

Open area test site; TEM cell; EMI test shielded chamber and shielded ferrite lined anechoic chamber; Tx /Rx Antennas, Sensors, Injectors / Couplers, and coupling factors; EMI Rx and spectrum analyzer; Civilian standards-CISPR, FCC, IEC, EN; Military standards-MIL461E/462.

TOTAL:45 PERIODS

COURSE OUTCOMES:

CO1: Gain enough knowledge to understand the concept of EMI / EMC related to product design & development.
CO2: To analyze the different EM coupling principles and its impact on performance of electronic system.
CO3: Analyze electromagnetic interference, highlighting the concepts of both susceptibility and immunity
CO4: Interpret various EM compatibility issues with regard to the design of pcbs and ways to improve the overall system performance
CO5: To obtain broad knowledge of various EM radiation measurement techniques and the present leading edge industry standards in different countries

REFERENCES:

1. V.P.Kodali, “Engineering EMC Principles, Measurements and Technologies”, IEEE Press, Newyork, 1996.
2. Henry W.Ott.,”Noise Reduction Techniques in Electronic Systems”, A Wiley Inter Science Publications, John Wiley and Sons, Newyork, 1988.
3. Bemhard Keiser, “Principles of Electromagnetic Compatibility”, Artech house, Norwood, 3rd Edition, 1986.
4. C.R.Paul,”Introduction to Electromagnetic Compatibility” , John Wiley and Sons, Inc, 1992.
5. Don R.J.White Consultant Incorporate, “Handbook of EMI/EMC” , Vol I-V, 1988.

	PO1	PO2	PO3	PO4	PO5	PO6
CO1			2			
CO2	1				3	3
CO3			2			
CO4			2	3	2	3
CO5					3	2
CO6				3	1	

VL5001 HARDWARE SOFTWARE CO-DESIGN L T P C
3 0 0 3

OBJECTIVES:

- To acquire the knowledge about system specification and modelling
- To learn the formulation of partitioning
- To study the different technical aspects about prototyping and emulation

UNIT I SYSTEM SPECIFICATION AND MODELLING 9

Embedded Systems, Hardware/Software Co-Design, Co-Design for System Specification and Modeling, Co-Design for Heterogeneous implementation - Processor Synthesis, Single-Processor Architectures with one ASIC, Single-Processor Architectures with many ASICs, Multi-Processor Architectures, Comparison of Co-Design approaches, Models of Computation, Requirements for Embedded System Specification.

UNIT II HARDWARE/SOFTWARE PARTITIONING 9

The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of the Partitioning Graph, Formulation of the HW/SW Partitioning Problem, Optimization, HW/SW Partitioning based on Heuristic Scheduling, HW/SW Partitioning based on Genetic Algorithms.

UNIT III HARDWARE/SOFTWARE CO-SYNTHESIS 9

The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis.

UNIT IV PROTOTYPING AND EMULATION 9

Introduction, Prototyping and Emulation Techniques, Prototyping and Emulation Environments, Future Developments in Emulation and Prototyping, Target Architecture, Architecture Specialization Techniques, System Communication Infrastructure, Target Architectures and Application System Classes, Architectures for Control-Dominated Systems, Architectures for Data-Dominated Systems, Mixed Systems and Less Specialized Systems.

UNIT V DESIGN SPECIFICATION AND VERIFICATION 9

Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification, Languages for System-Level Specification and Design System-Level Specification, Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specification and Multi-Language Co-simulation.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

CO1: Describe the broad range of system architectures and design methodologies that currently exist and define their fundamental attributes.

CO2: Discuss the dataflow models as a state-of-the-art methodology to solve co-design problems and to optimize the balance between software and hardware.

CO3: Understand in translating between software and hardware descriptions through co-design methodologies.

CO4: Understand the state-of-the-art practices in developing co-design solutions to problems using modern hardware/software tools for building prototypes.

CO5: Understand the concurrent specification from an algorithm, analyze its behavior and partition the specification into software (C code) and hardware (HDL) components

REFERENCES:

1. Patrick Schaumont, “A Practical Introduction to Hardware/Software Codesign”, Springer,2010.
2. Ralf Niemann, “Hardware/Software Co-Design for Data Flow Dominated Embedded Systems”, Kluwer Academic Publisher, 1998.
3. Jorgen Staunstrup, Wayne Wolf, “Hardware/Software Co-Design: Principles and Practice”, Kluwer Academic Publisher,1997.
4. Giovanni De Micheli, Rolf Ernst Morgon, “Reading in Hardware/Software Co-Design”, Kaufmann Publisher,2001.

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	----	2	1	3	1	--
CO2	3	2	1	---	1	---
CO3	1	3	2	----	----	1
CO4	3	2	----	3	----	----
CO5	----	3	----	1	---	1

VL5002 RECONFIGURABLE COMPUTING L T P C
3 0 0 3

OBJECTIVES:

- To study about the reconfigurable computing architectures
- Understand the concepts of software flexibility and hardware performance
- Usage of high speed computing fabrics like field-programmable gate arrays (FPGAs) and application-specific integrated circuits (ASICs)
- Design and applications of dynamic and partial reconfigurable computing systems

UNIT I RECONFIGURABLE COMPUTING HARDWARE 9

Domain specific processors, Application specific processors, Reconfigurable Computing Systems, Evolution of reconfigurable systems, Characteristics of RCS, advantages and issues. Device Architecture, Reconfigurable Computing Architectures, Reconfigurable Computing Systems, Reconfiguration Management

UNIT II PROGRAMMING RECONFIGURABLE SYSTEMS 9

Compute Models and System Architectures, Programming FPGA Applications in Verilog HDL, Compiling C for Spatial Computing, Programming Streaming FPGA Applications Using Block Diagrams in Simulink, Programming Data Parallel FPGA Applications, Operating System Support for Reconfigurable Computing, The JHDL Design and Debug System

UNIT III MAPPING DESIGNS TO RECONFIGURABLE PLATFORMS 9

Technology Mapping, Placement for General-purpose FPGAs, Datapath Composition, Specifying Circuit Layout on FPGAs, PathFinder: A Negotiation-based, Performance-driven Router for FPGAs, Retiming, Repipelining, and C-slow Retiming, Configuration Bitstream Generation, Fast Compilation Techniques

UNIT IV APPLICATION DEVELOPMENT 9

Implementing Applications with FPGAs, Instance-specific Design, Precision Analysis for Fixed-point Computation, Distributed Arithmetic, CORDIC Architectures for FPGA Computing, Hardware/Software Partitioning

UNIT V CASE STUDIES OF FPGA APPLICATIONS 9

SPIHT Image Compression, Automatic Target Recognition Systems on Reconfigurable Devices, Multi-FPGA Systems: Logic Emulation, The Implications of Floating Point for FPGAs, Evolvable FPGAs, Network Packet Processing in Reconfigurable Hardware, Active Pages: Memory-centric Computation

TOTAL: 45 PERIODS

COURSE OUTCOMES:

CO1: Understand the fundamentals of the reconfigurable computing and reconfigurable architectures.

CO2: Articulate the design issues involved in reconfigurable computing systems with a specific focus on Field Programmable Gate Arrays (FPGAs) both in theoretical and application levels.

CO3: Understand the performance trade-offs involved in designing a reconfigurable computing platform with a specific focus on the architecture of a configurable logic block and the programmable interconnect.

CO4: Discuss the state of the art reconfigurable computing architectures spanning fine grained (look up table based processing elements) to coarse grained (arithmetic logic unit level processing elements) architectures.

CO5: Understand both how to architect reconfigurable systems and how to utilize them for solving challenging computational problems.

REFERENCES:

1. Scott Hauck and Andre` DeHon, “Reconfigurable Computing: The Theory and Practice of FPGA-Based Computation”, Morgan Kaufmann, 2008.
2. Stephen M. Trimberger, “Field – programmable Gate Array Technology”, Springer, 2007.
3. CliveMaxfield, “The Design Warrior’s Guide to FPGAs: Devices, Tools and Flows”, Newnes, Elsevier, 2006.

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	1		1		
CO2	2		2		1	
CO3	1	3				
CO4		1			2	
CO5		2	2	1		

VL5003 EVOLVABLE HARDWARE L T P C
3 0 0 3

OBJECTIVES:

- To study about the Evolvable Systems algorithms, multi-objective utility functions
- Understand the concepts of reliability, design-in redundancy, fault tolerance and defect tolerance
- Design of evolvable systems using programmable logic devices (like FPGAs) and modular subsystems with identical components and generalized controller algorithms

UNIT I INTRODUCTION 9

Traditional hardware systems and its Limitations, Evolvable hardware, Characteristics of evolvable circuits and systems, Technology-Extrinsic and intrinsic evolution Offline and online evolution, Applications and scope of EHW

UNIT II EVOLUTIONARY COMPUTATION 9

Fundamentals of Evolutionary algorithms, Components of EA, Variants of EA, Genetic algorithms, Genetic Programming, Evolutionary strategies, Evolutionary programming, Implementations – Evolutionary design and optimizations, EHW – Current problems and potential solutions

UNIT III RECONFIGURABLE DIGITAL DEVICES 9

Basic architectures – Programmable Logic Devices, Field Programmable Gate Arrays (FPGAs), Using reconfigurable hardware – Design phase, Execution phase, Evolution of digital circuits

UNIT IV RECONFIGURABLE ANALOG DEVICES 9

Basic architectures – Field Programmable Transistor arrays (FPTAs), Analog arrays, MWMs, Using reconfigurable hardware – Design phase, Execution phase, Evolution of analog circuits

UNIT V APPLICATIONS OF EHW 9

Synthesis vs. adaptation, Designing self-adaptive systems, Fault-tolerant systems, Real-time systems, intrinsic reconfiguration for online systems, EHW based fault recovery and future work

TOTAL: 45 PERIODS

COURSE OUTCOMES:

CO1: Understand the fundamentals of computational models and computers which have appeared at the intersection of hardware and artificial intelligence to solve hard computational problems.

CO2: Understand the principles of bio-inspired and unconventional computational systems.

CO3: Discuss about the reconfigurable digital architectures and its computational intelligence techniques.

CO4: Discuss about the reconfigurable analog architectures and its computational intelligence techniques.

CO5: Discuss about the typical applications of bio-inspired and other unconventional techniques in the phase of design, implementation and runtime of a computational device.

REFERENCES:

1. Garrison W. Greenwood and Andrew M. Tyhrrell, “Introduction to Evolvable Hardware: A Practical Guide for Designing Self- Adaptive Systems”, Wiley-IEEE Press, 2006.
2. Tetsuya Higuchi, Xin Yao and Yong Liu, “Evolvable Hardware”, Springer-Verlag, 2004.
3. Lukas Sekanina, “Evolvable Components: From Theory to Hardware Implementations”, Springer, 2004.

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1		3		
CO2	1	1				
CO3	1	3				
CO4	3		2			
CO5		1				

VL5004 POWER MANAGEMENT AND CLOCK DISTRIBUTION CIRCUITS L T P C
3 0 0 3

OBJECTIVES:

- To teach the design of reference circuits and low drop out regulators for desired specifications
- To teach oscillator choice and requirements for clock generation circuits
- To teach the design of clock generation and recovery in the context of high speed systems

UNIT I VOLTAGE AND CURRENT REFERENCES 9

Current Mirrors, Self Biased Current Reference, startup circuits, VBE based Current Reference, VT Based Current Reference, Band Gap Reference , Supply Independent Biasing, Temperature Independent Biasing, PTAT Current Generation, Constant Gm Biasing

UNIT II LOW DROP OUT REGULATORS 9

Analog Building Blocks, Negative Feedback, Performance Metrics, AC Design, Stability, Internal and External Compensation, PSRR – Internal and External compensation circuits.

UNIT III OSCILLATOR FUNDAMENTALS 9

General considerations, Ring oscillators, LC oscillators, Colpitts Oscillator, Jitter and Phase noise in Ring Oscillators, Impulse Sensitivity Function for LC & Ring Oscillators, Phase Noise in Differential LC Oscillators.

UNIT IV CLOCK DISTRIBUTION CIRCUITS 9

PLL Fundamental, PLL stability, Noise Performance, Charge-Pump PLL Topology, CPPLL Building blocks, Jitter and Phase Noise performance, DLL fundamentals.

UNIT V CLOCK AND DATA RECOVERY CIRCUITS 9

CDR Architectures, Trans Impedance Amplifiers and Limiters, CMOS Interface, Linear Half Rate CMOS CDR Circuits, Wide capture Range CDR Circuits.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

CO1: Design Band gap reference circuits and Low Drop Out regulator for a given specification.
CO2: Understand specification related to Supply and Clock generation circuits of ICs
CO3: Choose oscillator topology and design meeting the requirement of clock generation circuits.
CO4: Design clock generation circuits in the context of high speed I/Os, High speed Broad
CO5: Band Communication circuits and Data Conversion Circuits.

REFERENCES:

1. Gabriel.A. Rincon-Mora, "Voltage references from diode to precision higher order bandgapcircuits", Johnwiley& Sons Inc, 2002.
2. Gabriel.A. Rincon-Mora, "Analog IC Design With Low-Dropout Regulators", McGraw-Hill Professional Pub, 2009.
3. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill, 2001
4. Floyd M. Gardner ,"Phase LocK Techniques" John wiley& Sons, Inc 2005.
5. Michiel Steyaert, Arthur H.M. van Roermund, Herman Casier, "Analog Circuit Design: High Speed Clock and Data Recovery, High-performance Amplifiers Power Management", springer, 2008.
6. BehzadRazavi, "Design of Integrated circuits for Optical Communications", McGraw Hill, 2003.

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		3	1	2	2
CO2	3		3	1	2	2
CO3	3		3	1	2	2
CO4	3		3	1	2	2
CO5	3		3	1	2	2

VL5005 TESTING OF VLSI CIRCUITS L T P C
3 0 0 3

OBJECTIVES:

- To introduce the VLSI Testing.
- To introduce Logic and Fault Simulation and Testability Measures.
- To study the Test Generation for Combinational and Sequential Circuits,
- To study the Design for Testability.
- To study the Fault Diagnosis

UNIT I INTRODUCTION TO TESTING 9

Introduction – VLSI Testing Process and Test Equipment – Challenges in VLSI Testing - Test Economics and Product Quality – Fault Modeling – Relationship among Fault Models.

UNIT II LOGIC &FAULT SIMULATION & TESTABILITY MEASURES 9

Simulation for Design Verification and Test Evaluation – Modeling Circuits for Simulation – Algorithms for True Value and Fault Simulation – SCOAP Controllability and Observability.

UNIT III TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS 9

Algorithms and Representations – Redundancy Identification – Combinational ATPG Algorithms – Sequential ATPG Algorithms – Simulation Based ATPG – Genetic Algorithm Based ATPG.

UNIT IV DESIGN FOR TESTABILITY 9

Design for Testability Basics – Testability Analysis - Scan Cell Designs – Scan Architecture – Built-In Self-Test – Random Logic BIST – DFT for other Test Objectives.

UNIT V FAULT DIAGNOSIS 9

Introduction and Basic Definitions – Fault Models for Diagnosis – Generation for Vectors for Diagnosis – Combinational Logic Diagnosis - Scan Chain Diagnosis – Logic BIST Diagnosis.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

CO1: Understand VLSI Testing Process.
CO2: Develop Logic Simulation and Fault Simulation.
CO3: Develop Test for Combinational and Sequential Circuits.
CO4: Understand the Design for Testability.
CO5: Perform Fault Diagnosis.

REFERENCES:

1. Laung-Terng Wang, Cheng-Wen Wu and Xiaoqing Wen, “VLSI Test Principles and Architectures”, Elsevier, 2017.
2. Michael L. Bushnell and Vishwani D. Agrawal, “Essentials of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits” , Kluwer Academic Publishers, 2017.
3. Niraj K. Jha and Sandeep Gupta, “Testing of Digital Systems”, Cambridge University Press, 2017.

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2		3			
CO2	2		3			
CO3	2		3			
CO4	2		3			
CO5	2		3			

VL5006 **SoC DESIGN** **L T P C**
3 0 0 3

OBJECTIVES:

- To understand the formulation of SoC based designs
- To teach SoC based design approaches
- To teach low power SoC design approaches

UNIT I ASIC **9**

Overview of ASIC types, design strategies, CISC, RISC and NISC approaches for SOC , architectural issues and its impact on SoC design methodologies, Application Specific Instruction Processor (ASIP) concepts.

UNIT II NISC **9**

NISC Control Words methodology, NISC Applications & Advantages, Architecture, Description Languages (ADL) for design and verification of Application Specific Instruction set Processors (ASIP), No-Instruction-Set-computer (NISC)- design flow, modelling NISC architectures and systems, use of Generic Netlist Representation - A formal language for specification, compilation and synthesis of embedded processors.

UNIT III SIMULATION **9**

Different simulation modes, behavioural, functional, static timing, gate level, switch level, transistor/circuit simulation, design of verification vectors, Low power FPGA, Reconfigurable systems, SoC related modeling of data path design and control logic, Minimization of interconnects impact, clock tree design issues.

UNIT IV LOW POWER SOC DESIGN / DIGITAL SYSTEM **9**

- Design synergy, Low power system perspective- power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimization, building block memory, power down techniques, power consumption verification.

UNIT V SYNTHESIS **9**

- Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trails paths, connectivity, components, mapping/visualization, nodal and admittance graph.Technology independent and technology dependent approaches for synthesis, optimization constraints, Synthesis report analysis, Single core and Multi core systems, dark silicon issues, HDL coding techniques for minimization of power consumption, Fault tolerant designs

TOTAL: 45 PERIODS

COURSE OUTCOMES:

CO1: Identify & formulate a given problem in framework of SoC based design approaches
CO2: Design SoC based system for engineering applications
CO3: Realize impact of SoC on electronic design philosophy and Macro-electronics thereby incline towards entrepreneurship & skill development.

REFERENCES:

1. Hubert Kaeslin, “Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication”, Cambridge University Press, 2008.
2. B. Al Hashimi, “System on chip-Next generation electronics”, The IET, 2006.
3. RochitRajsuman, “System-on- a-chip: Design and test”, Advantest America R & D Center, 2000.
4. P Mishra and N Dutt, “Processor Description Languages”, Morgan Kaufmann, 2008.
5. Michael J. Flynn and Wayne Luk, “Computer System Design: System-on-Chip”, Wiley, 2011.

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		3	1	3	3
CO2	3		3	1	3	3
CO3	3		3	1	3	3
CO4	3		3	1	3	3
CO5	3		3	1	3	3

VL5007 DATA CONVERTERS L T P C
3 0 0 3

OBJECTIVES:

- To teach A to D and D to A characteristics
- To teach the design of switched capacitor based circuits
- To teach the design of A/D and D/A converters

UNITI INTRODUCTION & CHARACTERISTICS OF AD/DA CONVERTER CHARACTERISTICS 9

Evolution, types and applications of AD/DA characteristics, issues in sampling, quantization and reconstruction, oversampling and antialiasing filters.

UNIT II SWITCH CAPACITOR CIRCUITS AND COMPARATORS 9

Switched-capacitor amplifiers, switched capacitor integrator, switched capacitor common mode feedback. Single stage amplifier as comparator, cascaded amplifier stages as comparator, latched comparators. offset cancellation, Op Amp offset cancellation, Calibration techniques

UNIT III NYQUIST RATE D/A CONVERTERS 9

Current Steering DACs, capacitive DACs, Binary weighted versus thermometer DACs, issues in current element matching, clock feed through, zero order hold circuits, DNL, INL and other performance metrics of ADCs and DACs

UNIT IV PIPELINE AND OTHER ADCs 9

Performance metrics, Flash architecture, Pipelined Architecture, Successive approximation architecture, Time interleaved architecture.

UNIT V SIGMA DELTA CONVERTERS 9

STF, NTF, first order and second order sigma delta modulator characteristics, Estimating the maximum stable amplitude, CTDSMs, Opamp nonlinearities

TOTAL : 45 PERIODS

COURSE OUTCOMES:

CO1: Ability to carry out the design calculations for developing the various blocks associated with a typical CMOS AD or DA converter.
CO2: Ability to design and implement circuits using switched capacitor concepts
CO3: Ability to analyze and design D/A converters
CO4: Ability to design different types of A/Ds
CO5: Ability to analyze and design sigma delta converters

REFERENCES:

1. Shanthi Pavan, Richard Schreier, Gabor C. Temes , "Understanding Delta-Sigma Data Converters", Willey –IEEE Press, 2nd Edition, 2017.
2. Behzad Razavi, "Principles of data conversion system design", IEEE press, 1995.
3. M. Pelgrom, "Analog-to-Digital Conversion", Springer, 2010.
4. Rudy van de Plassche, "CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters" Kluwer Acedamic Publishers, Boston, 2003.
5. J. G. Proakis, D. G. Manolakis, "Digital Signal Processing Principles, Algorithms and Applications", Prentice Hall, 4th Edition, 2006.
6. VLSI Data Conversion Circuits EE658 recorded lectures available at http://www.ee.iitm.ac.in/~nagendra/videolecture

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		3	1	2	2
CO2	3		3	1	2	2
CO3	3		3	1	2	2
CO4	3		3	1	2	2
CO5	3		3	1	2	2

VL5008 CAD FOR VLSI CIRCUITS L T P C
3 0 0 3

OBJECTIVES:

- To introduce the VLSI Design Methodologies and Design Methods.
- To introduce Data Structures and Algorithms required for VLSI Design.
- To study Algorithms for Partitioning and Placement.
- To study Algorithms for Floor planning and Routing.
- To study Algorithms for Modelling, Simulation and Synthesis.

UNIT I INTRODUCTION 9

Introduction to VLSI Design Methodologies – VLSI Design Cycle – New Trends in VLSI Design Cycle – Physical Design Cycle – New Trends in Physical Design Cycle – Design Styles – Review of VLSI Design Automation Tools.

UNIT II DATA STRUCTURES AND BASIC ALGORITHMS 9

Introduction to Data Structures and Algorithms – Algorithmic Graph Theory and Computational Complexity – Tractable and Intractable Problems – General Purpose Methods for Combinatorial Optimization.

UNIT III ALGORITHMS FOR PARTITIONING AND PLACEMENT 9

Layout Compaction – Problem Formulation – Algorithms for Constraint Graph Compaction – Partitioning – Placement – Placement Algorithms.

UNIT IV ALGORITHMS FOR FLOORPLANNING AND ROUTING 9

Floorplanning – Problem Formulation – Floorplanning Algorithms – Routing – Area Routing – Global Routing – Detailed Routing.

UNIT V MODELLING, SIMULATION AND SYNTHESIS 9

Simulation – Gate Level Modeling and Simulation – Logic Synthesis and Verification – Binary Decision Diagrams – High Level Synthesis.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

CO1: Use various VLSI Design Methodologies and Design Methods.
CO2: Understand different Data Structures and Algorithms required for VLSI Design.
CO3: Develop Algorithms for Partitioning and Placement.
CO4: Develop Algorithms for Floorplanning and Routing.
CO5: Design Algorithms for Modelling, Simulation and Synthesis.

REFERENCES:

1. Sabih H. Gerez, “Algorithms for VLSI Design Automation”, Second Edition, Wiley-India, 2017.
2. Naveed A. Sherwani, “Algorithms for VLSI Physical Design Automation”, 3rd Edition, Springer, 2017.
3. Charles J. Alpert, Dinesh P. Mehta and Sachin S Sapatnekar, “Handbook of Algorithms for Physical Design Automation, CRC Press, 1st Edition, 2

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2		3			
CO2	2		3			
CO3	2		3			
CO4	2		3			
CO5	2		3			

VL5009 VLSI SIGNAL PROCESSING L T P C
3 0 0 3

OBJECTIVES:

- To introduce techniques for altering existing DSP structures to suit VLSI implementations.
- To introduce efficient design of DSP architectures suitable for VLSI

UNIT I INTRODUCTION TO DSP SYSTEMS, PIPELINING AND PARALLEL PROCESSING OF FIR FILTERS 9

Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs - critical path, Loop bound, iteration bound, Longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.

UNIT II RETIMING, ALGORITHMIC STRENGTH REDUCTION 9

Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture, parallel rank-order filters.

UNIT III FAST CONVOLUTION, PIPELINING AND PARALLEL PROCESSING OF IIR FILTERS 9

Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with power- of-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

UNIT IV BIT-LEVEL ARITHMETIC ARCHITECTURES 9

Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon‟s bit-serial multipliers using Horner‟s rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner‟s rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters

UNIT V NUMERICAL STRENGTH REDUCTION, SYNCHRONOUS, WAVE AND ASYNCHRONOUS PIPELINING 9

Numerical strength reduction – sub expression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol.

TOTAL : 45 PERIODS

COURSE OUTCOMES:

CO1: Ability to determine the parameters influencing the efficiency of DSP architectures and apply pipelining and parallel processing techniques to alter FIR structures for efficiency

CO2: Ability to analyse and modify the design equations leading to efficient DSP architectures for transforms

CO3: Ability to speed up convolution process and develop fast and area efficient IIR structures

CO4: Ability to develop fast and area efficient multiplier architectures

CO5: Ability to reduce multiplications and build fast hardware for synchronous digital systems

REFERENCES

1. Keshab K. Parhi, " VLSI Digital Signal Processing Systems, Design and implementation ", Wiley, Interscience, 2007.
2. U. Meyer – Baese, " Digital Signal Processing with Field Programmable Gate Arrays", Springer, 2nd Edition, 2004.

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		2			
CO2	3		2			
CO3	3		2			
CO4	3		3			
CO5	3		3			

AP5251 ADVANCED DIGITAL SYSTEM DESIGN L T P C
3 0 0 3

OBJECTIVES:

- To introduce methods to analyse and design synchronous sequential circuits
- To introduce methods to analyse and design asynchronous sequential circuits and to analyse hazards
- To introduce the fault testing procedure for combinational circuits and PLA circuits
- To introduce the architectures of programmable devices
- To introduce design and implementation of digital circuits using programming tools

UNIT I SEQUENTIAL CIRCUIT DESIGN 9

Analysis of clocked synchronous sequential circuits and modelling- State diagram, state table, state table assignment and reduction-Design of synchronous sequential circuits design of iterative circuits-ASM chart and realization using ASM

UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 9

Analysis of asynchronous sequential circuit – flow table reduction-races-state assignment-transition table and problems in transition table- design of asynchronous sequential circuit-Static, dynamic and essential hazards – mixed operating mode asynchronous circuits – designing vending machine controller

UNIT III FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS 9

Fault table method-path sensitization method – Boolean difference method - D algorithm – Kohavi algorithm – Tolerance techniques – The compact algorithm – Fault in PLA – Test generation-DFT schemes – Built in self test

UNIT IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES 9

Programming logic device families – Designing a synchronous sequential circuit using PLA/PAL – Designing ROM with PLA – Realization of finite state machine using PLD – FPGA – Xilinx FPGA-Xilinx 4000

UNIT V SYSTEM DESIGN USING VERILOG 9

Hardware Modelling with Verilog HDL – Logic System, Data Types and Operators For Modelling in Verilog HDL - Behavioural Descriptions in Verilog HDL – HDL Based Synthesis – Synthesis of Finite State Machines– structural modelling – compilation and simulation of Verilog code –Test bench - Realization of combinational and sequential circuits using Verilog – Registers – counters – sequential machine – serial adder – Multiplier- Divider – Design of simple microprocessor

TOTAL: 45 PERIODS

COURSE OUTCOMES:

CO1: Analyse and design synchronous sequential circuits
CO2: Analyse hazards and design asynchronous sequential circuits
CO3; Knowledge on the testing procedure for combinational circuit and PLA
CO4: Able to design PLD and ROM
CO5: Design and use programming tools for implementing digital circuits of industry standards

REFERENCES:

1. Charles H.RothJr “Fundamentals of Logic Design” Thomson Learning 2004
2. M.D.Ciletti , Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Prentice Hall, 1999
3. M.G.Arnold, Verilog Digital – Computer Design, Prentice Hall (PTR), 1999.
4. Nripendra N Biswas “Logic Design Theory” Prentice Hall of India,2001
5. ParagK.Lala “Fault Tolerant and Fault Testable Hardware Design” B S
6. Publications,2002
7. ParagK.Lala “Digital system Design using PLD” B S Publications,2003
8. S. Palnitkar , Verilog HDL – A Guide to Digital Design and Synthesis, Pearson , 2003.

	PO1	PO2	PO3	PO4	PO5	PO6
CO1			2			
CO2			2			
CO3	3			3	1	
CO4					2	
CO5				2		

OE5091 BUSINESS DATA ANALYTICS L T P C
3 0 0 3

OBJECTIVES:

- To understand the basics of business analytics and its life cycle.
- To gain knowledge about fundamental business analytics.
- To learn modeling for uncertainty and statistical inference.
- To understand analytics using Hadoop and Map Reduce frameworks.
- To acquire insight on other analytical frameworks.

UNIT I OVERVIEW OF BUSINESS ANALYTICS 9

Introduction – Drivers for Business Analytics – Applications of Business Analytics: Marketing and Sales, Human Resource, Healthcare, Product Design, Service Design, Customer Service and Support – Skills Required for a Business Analyst – Framework for Business Analytics Life Cycle for Business Analytics Process.

Suggested Activities:

- Case studies on applications involving business analytics.
- Converting real time decision making problems into hypothesis.
- Group discussion on entrepreneurial opportunities in Business Analytics.

Suggested Evaluation Methods:

- Assignment on business scenario and business analytical life cycle process.
- Group presentation on big data applications with societal need.
- Quiz on case studies.

UNIT II ESSENTIALS OF BUSINESS ANALYTICS 9

Descriptive Statistics – Using Data – Types of Data – Data Distribution Metrics: Frequency, Mean, Median, Mode, Range, Variance, Standard Deviation, Percentile, Quartile, z-Score, Covariance, Correlation – Data Visualization: Tables, Charts, Line Charts, Bar and Column Chart, Bubble Chart, Heat Map – Data Dashboards.

Suggested Activities:

- Solve numerical problems on basic statistics.
- Explore chart wizard in MS Excel Case using sample real time data for data visualization.
- Use R tool for data visualization.

Suggested Evaluation Methods:

- Assignment on descriptive analytics using benchmark data.
- Quiz on data visualization for univariate, bivariate data.

UNIT III MODELING UNCERTAINTY AND STATISTICAL INFERENCE 9

Modeling Uncertainty: Events and Probabilities – Conditional Probability – Random Variables – Discrete Probability Distributions – Continuous Probability Distribution – Statistical Inference: Data Sampling – Selecting a Sample – Point Estimation – Sampling Distributions – Interval Estimation – Hypothesis Testing.

Suggested Activities:

- Solving numerical problems in sampling, probability, probability distributions and hypothesis testing.
- Converting real time decision making problems into hypothesis.

Suggested Evaluation Methods:

- Assignments on hypothesis testing.
- Group presentation on real time applications involving data sampling and hypothesis testing.
- Quizzes on topics like sampling and probability.

UNIT IV ANALYTICS USING HADOOP AND MAPREDUCE FRAMEWORK 9

Introducing Hadoop – RDBMS versus Hadoop – Hadoop Overview – HDFS (Hadoop Distributed File System) – Processing Data with Hadoop – Introduction to MapReduce – Features of MapReduce – Algorithms Using Map-Reduce: Matrix-Vector Multiplication, Relational Algebra Operations, Grouping and Aggregation – Extensions to MapReduce.

Suggested Activities:

- Practical – Install and configure Hadoop.
- Practical – Use web based tools to monitor Hadoop setup.
- Practical – Design and develop MapReduce tasks for word count, searching involving text corpus etc.

Suggested Evaluation Methods:

- Evaluation of the practical implementations.
- Quizzes on topics like HDFS and extensions to MapReduce.

UNIT V OTHER DATA ANALYTICAL FRAMEWORKS 9

Overview of Application development Languages for Hadoop – PigLatin – Hive – Hive Query Language (HQL) – Introduction to Pentaho, JAQL – Introduction to Apache: Sqoop, Drill and Spark, Cloudera Impala – Introduction to NoSQL Databases – Hbase and MongoDB.

Suggested Activities:

- Practical – Installation of NoSQL database like MongoDB.
- Practical – Demonstration on Sharding in MongoDB.
- Practical – Install and run Pig
- Practical – Write PigLatin scripts to sort, group, join, project, and filter data.
- Design and develop algorithms to be executed in MapReduce involving numerical methods for analytics.

Suggested Evaluation Methods:

- Mini Project (Group) – Real time data collection, saving in NoSQL, implement analytical techniques using Map-Reduce Tasks and Result Projection.

TOTAL: 45 PERIODS

COURSE OUTCOMES:
On completion of the course, the student will be able to:

- Identify the real world business problems and model with analytical solutions.
- Solve analytical problem with relevant mathematics background knowledge.
- Convert any real world decision making problem to hypothesis and apply suitable statistical testing.
- Write and Demonstrate simple applications involving analytics using Hadoop and MapReduce
- Use open source frameworks for modeling and storing data.
- Apply suitable visualization technique using R for visualizing voluminous data.

REFERENCES:

1. Vignesh Prajapati, “Big Data Analytics with R and Hadoop”, Packt Publishing, 2013.
2. Umesh R Hodeghatta, Umesha Nayak, “Business Analytics Using R – A Practical Approach”, Apress, 2017.
3. Anand Rajaraman, Jeffrey David Ullman, “Mining of Massive Datasets”, Cambridge University Press, 2012.
4. Jeffrey D. Camm, James J. Cochran, Michael J. Fry, Jeffrey W. Ohlmann, David R. Anderson, “Essentials of Business Analytics”, Cengage Learning, second Edition, 2016.
5. U. Dinesh Kumar, “Business Analytics: The Science of Data-Driven Decision Making”, Wiley, 2017.
6. A. Ohri, “R for Business Analytics”, Springer, 2012
7. Rui Miguel Forte, “Mastering Predictive Analytics with R”, Packt Publication, 2015.

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1	1	1	2	3	1
CO2	2	1	1	2	1	1
CO3	1	1	2	3	3	1
CO4	2	2	1	2	1	1
CO5	1	1	2	2	1	1
CO6	1	1	1	3	2	1

OE5092 **INDUSTRIAL SAFETY** **L T P C**
3 0 0 3

OBJECTIVES:

- Summarize basics of industrial safety
- Describe fundamentals of maintenance engineering
- Explain wear and corrosion
- Illustrate fault tracing
- Identify preventive and periodic maintenance

UNIT I INTRODUCTION **9**

Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc, Safety color codes. Fire prevention and firefighting, equipment and methods.

UNIT II FUNDAMENTALS OF MAINTENANCE ENGINEERING 9

Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy, Service life of equipment.

UNIT III WEAR AND CORROSION AND THEIR PREVENTION 9

Wear- types, causes, effects, wear reduction methods, lubricants-types and applications, Lubrication methods, general sketch, working and applications, i. Screw down grease cup, ii. Pressure grease gun, iii. Splash lubrication, iv. Gravity lubrication, v. Wick feed lubrication vi. Side feed lubrication, vii. Ring lubrication, Definition, principle and factors affecting the corrosion. Types of corrosion, corrosion prevention methods.

UNIT IV FAULT TRACING 9

Fault tracing-concept and importance, decision tree concept, need and applications, sequence of fault finding activities, show as decision tree, draw decision tree for problems in machine tools, hydraulic, pneumatic, automotive, thermal and electrical equipment's like, I. Any one machine tool, ii. Pump iii. Air compressor, iv. Internal combustion engine, v. Boiler, vi. Electrical motors, Types of faults in machine tools and their general causes.

UNIT V PERIODIC AND PREVENTIVE MAINTENANCE 9

Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components, overhauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance. Steps/procedure for periodic and preventive maintenance of: I. Machine tools, ii. Pumps, iii. Air compressors, iv. Diesel generating (DG) sets, Program and schedule of preventive maintenance of mechanical and electrical equipment, advantages of preventive maintenance. Repair cycle concept and importance

TOTAL: 45 PERIODS

COURSE OUTCOMES:

Students will be able to:

CO1: Ability to summarize basics of industrial safety

CO2: Ability to describe fundamentals of maintenance engineering

CO3: Ability to explain wear and corrosion

CO4: Ability to illustrate fault tracing

CO5: Ability to identify preventive and periodic maintenance

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	✓											
CO2	✓											
CO3	✓	✓	✓									
CO4	✓	✓	✓									
CO5	✓	✓	✓									

REFERENCES:

1. Audels, Pump-hydraulic Compressors, Mcgrew Hill Publication, 1978.
2. Garg H P,Maintenance Engineering, S. Chand and Company,1987.
3. Hans F. Winterkorn, Foundation Engineering Handbook, Chapman & Hall London, 2013.
4. Higgins & Morrow, Maintenance Engineering Handbook, Eighth Edition,2008

OE5093 **OPERATIONS RESEARCH** **L T P C**
3 0 0 3

OBJECTIVES:

- Solve linear programming problem and solve using graphical method.
- Solve LPP using simplex method
- Solve transportation, assignment problems
- Solve project management problems
- Solve scheduling problems

UNIT I LINEAR PROGRAMMING 9

Introduction to Operations Research – assumptions of linear programming problems - Formulations of linear programming problem – Graphical method

UNIT II ADVANCES IN LINEAR PROGRAMMING 9

Solutions to LPP using simplex algorithm- Revised simplex method - primal dual relationships – Dual simplex algorithm - Sensitivity analysis

UNIT III NETWORK ANALYSIS – I 9

Transportation problems -Northwest corner rule, least cost method, Voges's approximation method - Assignment problem -Hungarian algorithm

UNIT IV NETWORK ANALYSIS – II 9

Shortest path problem: Dijkstra's algorithms, Floyds algorithm, systematic method -CPM/PERT

UNIT V NETWORK ANALYSIS – III 9

Scheduling and sequencing - single server and multiple server models - deterministic inventory models - Probabilistic inventory control models

TOTAL: 45 PERIODS

COURSE OUTCOMES:

Students will be able to:

CO1: To formulate linear programming problem and solve using graphical method.

CO2: To solve LPP using simplex method

CO3: To formulate and solve transportation, assignment problems

CO4: To solve project management problems

CO5: To solve scheduling problems

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	✓											
CO2	✓											
CO3	✓	✓	✓									
CO4	✓	✓	✓									
CO5	✓	✓	✓									

REFERENCES:

1. Harvey M Wagner, Principles of Operations Research: Prentice Hall of India 2010
2. Hitler Libermann, Operations Research: McGraw Hill Pub. 2009
3. Pant J C, Introduction to Optimisation: Operations Research, Jain Brothers, Delhi, 2008
4. Pannerselvam, Operations Research: Prentice Hall of India 2010
5. Taha H A, Operations Research, An Introduction, PHI, 2008

OE5094 COST MANAGEMENT OF ENGINEERING PROJECTS L T P C
3 0 0 3

OBJECTIVES:

- Summarize the costing concepts and their role in decision making
- Infer the project management concepts and their various aspects in selection
- Interpret costing concepts with project execution
- Develop knowledge of costing techniques in service sector and various budgetary control techniques
- Illustrate with quantitative techniques in cost management

UNIT I INTRODUCTION TO COSTING CONCEPTS 9

Objectives of a Costing System; Cost concepts in decision-making; Relevant cost, Differential cost, Incremental cost and Opportunity cost; Creation of a Database for operational control.

UNIT II INTRODUCTION TO PROJECT MANAGEMENT 9

Project: meaning, Different types, why to manage, cost overruns centres, various stages of project execution: conception to commissioning. Project execution as conglomeration of technical and nontechnical activities, Detailed Engineering activities, Pre project execution main clearances and documents, Project team: Role of each member, Importance Project site: Data required with significance, Project contracts.

UNIT III PROJECT EXECUTION AND COSTING CONCEPTS 9

Project execution Project cost control, Bar charts and Network diagram, Project commissioning: mechanical and process, Cost Behavior and Profit Planning Marginal Costing; Distinction between Marginal Costing and Absorption Costing; Break-even Analysis, Cost-Volume-Profit Analysis, Various decision-making problems, Pricing strategies: Pareto Analysis, Target costing, Life Cycle Costing.

UNIT IV COSTING OF SERVICE SECTOR AND BUDGETERY CONTROL 9

Just-in-time approach, Material Requirement Planning, Enterprise Resource Planning, Activity-Based Cost Management, Bench Marking; Balanced Score Card and Value-Chain Analysis, Budgetary Control: Flexible Budgets; Performance budgets; Zero-based budgets.

UNIT V QUANTITATIVE TECHNIQUES FOR COST MANAGEMENT 9

Linear Programming, PERT/CPM, Transportation problems, Assignment problems, Learning Curve Theory.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

Students will be able to:

CO1 – Understand the costing concepts and their role in decision making

CO2–Understand the project management concepts and their various aspects in selection

CO3–Interpret costing concepts with project execution

CO4–Gain knowledge of costing techniques in service sector and various budgetary control techniques

CO5 - Become familiar with quantitative techniques in cost management

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	✓	✓	✓		✓			✓	✓		✓	✓
CO2	✓	✓	✓		✓				✓		✓	✓
CO3	✓	✓	✓		✓	✓					✓	✓
CO4	✓	✓	✓		✓		✓				✓	✓
CO5	✓	✓	✓		✓	✓	✓				✓	✓

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1.Ashish K. Bhattacharya, Principles & Practices of Cost Accounting A. H. Wheeler publisher, 1991
2. Charles T. Horngren and George Foster, Advanced Management Accounting, 1988
3. Charles T. Horngren et al Cost Accounting A Managerial Emphasis, Prentice Hall of India, New Delhi, 2011
4. Robert S Kaplan Anthony A. Alkinson, Management & Cost Accounting, 2003
5. Vohra N.D., Quantitative Techniques in Management, Tata McGraw Hill Book Co. Ltd, 2007

OE5095 COMPOSITE MATERIALS L T P C
3 0 0 3

OBJECTIVES:
- Summarize the characteristics of composite materials and effect of reinforcement in composite materials.
- Identify the various reinforcements used in composite materials.
- Compare the manufacturing process of metal matrix composites.
- Understand the manufacturing processes of polymer matrix composites.
- Analyze the strength of composite materials.

UNIT I INTRODUCTION 9
Definition – Classification and characteristics of Composite materials - Advantages and application of composites - Functional requirements of reinforcement and matrix - Effect of reinforcement (size, shape, distribution, volume fraction) on overall composite performance.

UNIT II REINFORCEMENTS 9
Preparation-layup, curing, properties and applications of glass fibers, carbon fibers, Kevlar fibers and Boron fibers - Properties and applications of whiskers, particle reinforcements - Mechanical Behavior of composites: Rule of mixtures, Inverse rule of mixtures - Isostrain and Isostress conditions.

UNIT III MANUFACTURING OF METAL MATRIX COMPOSITES 9
Casting – Solid State diffusion technique - Cladding – Hot isostatic pressing - Properties and applications. Manufacturing of Ceramic Matrix Composites: Liquid Metal Infiltration – Liquid phase sintering. Manufacturing of Carbon – Carbon composites: Knitting, Braiding, Weaving - Properties and applications.

UNIT IV MANUFACTURING OF POLYMER MATRIX COMPOSITES 9
Preparation of Moulding compounds and prepregs – hand layup method – Autoclave method – Filament winding method – Compression moulding – Reaction injection moulding - Properties and applications.

UNIT V STRENGTH 9
Laminar Failure Criteria-strength ratio, maximum stress criteria, maximum strain criteria, interacting failure criteria, hygrothermal failure. Laminate first play failure-insight strength; Laminate strength-ply discount truncated maximum strain criterion; strength design using caplet plots; stress concentrations.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

Students will be able to:

CO1 Know the characteristics of composite materials and effect of reinforcement in composite materials.

CO2 Know the various reinforcements used in composite materials.

CO3 Understand the manufacturing processes of metal matrix composites.

CO4 Understand the manufacturing processes of polymer matrix composites.

CO5 Analyze the strength of composite materials.

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1		✓	✓	✓								
CO2		✓	✓	✓	✓						✓	
CO3			✓	✓	✓		✓				✓	
CO4			✓	✓	✓		✓				✓	
CO5			✓	✓	✓		✓					

REFERENCES:

1. Cahn R.W. - Material Science and Technology – Vol 13 – Composites, VCH, West Germany.
2. Callister, W.D Jr., Adapted by Balasubramaniam R, Materials Science and Engineering, An introduction, John Wiley & Sons, NY, Indian edition, 2007.
3. Chawla K.K., Composite Materials, 2013.
4. Lubin.G, Hand Book of Composite Materials, 2013.

OE5096 WASTE TO ENERGY L T P C

3 0 0 3

OBJECTIVES:

- Interpret the various types of wastes from which energy can be generated
- Develop knowledge on biomass pyrolysis process and its applications
- Develop knowledge on various types of biomass gasifiers and their operations
- Invent knowledge on biomass combustors and its applications on generating energy
- Summarize the principles of bio-energy systems and their features

UNIT I INTRODUCTION TO EXTRACTION OF ENERGY FROM WASTE 9

Classification of waste as fuel – Agro based, Forest residue, Industrial waste - MSW – Conversion devices – Incinerators, gasifiers, digestors

UNIT II BIOMASS PYROLYSIS 9

Pyrolysis – Types, slow fast – Manufacture of charcoal – Methods - Yields and application – Manufacture of pyrolytic oils and gases, yields and applications.

UNIT III BIOMASS GASIFICATION 9

Gasifiers – Fixed bed system – Downdraft and updraft gasifiers – Fluidized bed gasifiers – Design, construction and operation – Gasifier burner arrangement for thermal heating – Gasifier engine arrangement and electrical power – Equilibrium and kinetic consideration in gasifier operation.

UNIT IV BIOMASS COMBUSTION 9

Biomass stoves – Improved chullahs, types, some exotic designs, Fixed bed combustors, Types, inclined grate combustors, Fluidized bed combustors, Design, construction and operation - Operation of all the above biomass combustors.

UNIT V BIO ENERGY 9

Properties of biogas (Calorific value and composition), Biogas plant technology and status - Bio energy system - Design and constructional features - Biomass resources and their classification - Biomass conversion processes - Thermo chemical conversion - Direct combustion - biomass gasification - pyrolysis and liquefaction - biochemical conversion - anaerobic digestion - Types of biogas Plants – Applications - Alcohol production from biomass - Bio diesel production - Urban waste to energy conversion - Biomass energy programme in India.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

Students will be able to:

CO1 Understand the various types of wastes from which energy can be generated
CO2 Gain knowledge on biomass pyrolysis process and its applications
CO3 Develop knowledge on various types of biomass gasifiers and their operations
CO4 Gain knowledge on biomass combustors and its applications on generating energy
CO5 Understand the principles of bio-energy systems and their features

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	✓		✓									✓
CO2	✓		✓									✓
CO3	✓	✓	✓		✓							✓
CO4	✓	✓	✓		✓		✓					✓
CO5	✓	✓	✓		✓							✓

REFERENCES:

1. Biogas Technology - A Practical Hand Book - Khandelwal, K. C. and Mahdi, S. S., Vol. I & II, Tata McGraw Hill Publishing Co. Ltd., 1983.
2. Biomass Conversion and Technology, C. Y. WereKo-Brobby and E. B. Hagan, John Wiley & Sons, 1996.
3. Food, Feed and Fuel from Biomass, Challal, D. S., IBH Publishing Co. Pvt. Ltd., 1991.
4. Non Conventional Energy, Desai, Ashok V., Wiley Eastern Ltd., 1990.

AUDIT COURSES (AC)

AX5091 ENGLISH FOR RESEARCH PAPER WRITING L T P C
2 0 0 0

OBJECTIVES

- Teach how to improve writing skills and level of readability
- Tell about what to write in each section
- Summarize the skills needed when writing a Title
- Infer the skills needed when writing the Conclusion
- Ensure the quality of paper at very first-time submission

UNIT I INTRODUCTION TO RESEARCH PAPER WRITING 6

Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

UNIT II PRESENTATION SKILLS 6

Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts, Introduction

UNIT III TITLE WRITING SKILLS 6

Key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check

UNIT IV RESULT WRITING SKILLS 6

Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions

UNIT V VERIFICATION SKILLS 6

Useful phrases, checking Plagiarism, how to ensure paper is as good as it could possibly be the first- time submission

TOTAL: 30 PERIODS

COURSE OUTCOMES

CO1 –Understand that how to improve your writing skills and level of readability
CO2 – Learn about what to write in each section
CO3 – Understand the skills needed when writing a Title
CO4 – Understand the skills needed when writing the Conclusion
CO5 – Ensure the good quality of paper at very first-time submission

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1										✓		✓
CO2										✓		✓
CO3										✓		✓
CO4										✓		✓
CO5										✓		✓

REFERENCES

1. Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011
2. Day R How to Write and Publish a Scientific Paper, Cambridge University Press 2006
3. Goldbort R Writing for Science, Yale University Press (available on Google Books) 2006
4. Highman N, Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book 1998.

AX5092 DISASTER MANAGEMENT L T P C
2 0 0 0

OBJECTIVES

- Summarize basics of disaster
- Explain a critical understanding of key concepts in disaster risk reduction and humanitarian response.
- Illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
- Describe an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
- Develop the strengths and weaknesses of disaster management approaches

UNIT I INTRODUCTION 6

Disaster: Definition, Factors and Significance; Difference between Hazard And Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

UNIT II REPERCUSSIONS OF DISASTERS AND HAZARDS 6

Economic Damage, Loss of Human and Animal Life, Destruction Of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts And Famines, Landslides And Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks And Spills, Outbreaks Of Disease And Epidemics, War And Conflicts.

UNIT III DISASTER PRONE AREAS IN INDIA 6

Study of Seismic Zones; Areas Prone To Floods and Droughts, Landslides And Avalanches; Areas Prone To Cyclonic and Coastal Hazards with Special Reference To Tsunami; Post-Disaster Diseases and Epidemics

UNIT IV DISASTER PREPAREDNESS AND MANAGEMENT 6

Preparedness: Monitoring Of Phenomena Triggering a Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological And Other Agencies, Media Reports: Governmental and Community Preparedness.

UNIT V RISK ASSESSMENT 6

Disaster Risk: Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival.

TOTAL : 30 PERIODS

COURSE OUTCOMES

CO1: Ability to summarize basics of disaster

CO2: Ability to explain a critical understanding of key concepts in disaster risk reduction and humanitarian response.

CO3: Ability to illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.

CO4: Ability to describe an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.

CO5: Ability to develop the strengths and weaknesses of disaster management approaches

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	✓											
CO2	✓											
CO3	✓	✓	✓									
CO4	✓	✓	✓									
CO5	✓	✓	✓									

REFERENCES

1. Goel S. L., Disaster Administration And Management Text And Case Studies",Deep & Deep Publication Pvt. Ltd., New Delhi,2009.
2. NishithaRai, Singh AK, "Disaster Management in India: Perspectives, issues and strategies "'NewRoyal book Company,2007.
3. Sahni, PardeepEt.Al. ," Disaster Mitigation Experiences And Reflections", Prentice Hall OfIndia, New Delhi,2001.

AX5093 SANSKRIT FOR TECHNICAL KNOWLEDGE L T P C
2 0 0 0

OBJECTIVES

- Illustrate the basic sanskrit language.
- Recognize sanskrit, the scientific language in the world.
- Appraise learning of sanskrit to improve brain functioning.
- Relate sanskrit to develop the logic in mathematics, science & other subjects enhancing the memory power.
- Extract huge knowledge from ancient literature.

UNIT I ALPHABETS 6

Alphabets in Sanskrit

UNIT II TENSES AND SENTENCES 6

Past/Present/Future Tense - Simple Sentences

UNIT III ORDER AND ROOTS 6

Order - Introduction of roots

UNIT IV SANSKRIT LITERATURE 6

Technical information about Sanskrit Literature

UNIT V TECHNICAL CONCEPTS OF ENGINEERING 6

Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics

TOTAL: 30 PERIODS

COURSE OUTCOMES

- CO1 - Understanding basic Sanskrit language.
- CO2 - Write sentences.
- CO3 - Know the order and roots of Sanskrit.
- CO4 - Know about technical information about Sanskrit literature.
- CO5 - Understand the technical concepts of Engineering.

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1										✓		✓
CO2										✓		✓
CO3												✓
CO4												✓
CO5												✓

REFERENCES

1. “Abhyaspustakam” – Dr. Vishwas, Samskrita-Bharti Publication, New Delhi
2. “Teach Yourself Sanskrit” Prathama Deeksha-Vempati Kutumbshastri, Rashtriya Sanskrit Sansthanam, New Delhi Publication
3. “India’s Glorious Scientific Tradition” Suresh Soni, Ocean books (P) Ltd., New Delhi, 2017.

AX5094 **VALUE EDUCATION** **L T P C**
2 0 0 0

OBJECTIVES
Students will be able to
- Understand value of education and self-development
- Imbibe good values in students
- Let the should know about the importance of character

UNIT I
Values and self-development–Social values and individual attitudes. Work ethics, Indian vision of humanism. Moral and non-moral valuation. Standards and principles. Value judgements

UNIT II
Importance of cultivation of values. Sense of duty. Devotion, Self-reliance. Confidence, Concentration. Truthfulness, Cleanliness. Honesty, Humanity. Power of faith, National Unity. Patriotism. Love for nature, Discipline

UNIT III
Personality and Behavior Development-Soul and Scientific attitude. Positive Thinking. Integrity and discipline. Punctuality, Love and Kindness. Avoid fault Thinking. Free from anger, Dignity of labour.
Universal brother hood and religious tolerance. True friendship. Happiness Vs suffering, love for truth. Aware of self-destructive habits. Association and Cooperation. Doing best for saving nature

UNIT IV
Character and Competence–Holy books vs Blind faith. Self-management and Good health. Science of reincarnation. Equality, Nonviolence, Humility, Role of Women. All religions and same message. Mind your Mind, Self-control. Honesty, Studying effectively.

TOTAL: 30 PERIODS

COURSE OUTCOMES
Students will be able to
- Knowledge of self-development.
- Learn the importance of Human values.
- Developing the overall personality.

SUGGESTED READING
1. Chakroborty, S.K."Values and Ethics for organizations Theory and practice", Oxford University Press, New Delhi

AX5095 **CONSTITUTION OF INDIA** **L T P C**
2 0 0 0

OBJECTIVES
Students will be able to:
- Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.
- To address the growth of Indian opinion regarding modern Indian intellectuals' constitutional
- Role and entitlement to civil and economic rights as well as the emergence nation hood in the early years of Indian nationalism.
- To address the role of socialism in India after the commencement of the Bolshevik Revolutionin1917and its impact on the initial drafting of the Indian Constitution.

UNIT I HISTORY OF MAKING OF THE INDIAN CONSTITUTION:
History, Drafting Committee, (Composition & Working)

UNIT II PHILOSOPHY OF THE INDIAN CONSTITUTION:
Preamble, Salient Features

UNIT III CONTOURS OF CONSTITUTIONAL RIGHTS AND DUTIES:
Fundamental Rights, Right to Equality, Right to Freedom, Right against Exploitation, Right to Freedom of Religion, Cultural and Educational Rights, Right to Constitutional Remedies, Directive Principles of State Policy, Fundamental Duties.

UNIT IV ORGANS OF GOVERNANCE:
Parliament, Composition, Qualifications and Disqualifications, Powers and Functions, Executive, President, Governor, Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualifications, Powers and Functions.

UNIT V LOCAL ADMINISTRATION:
District's Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CEO, Municipal Corporation. Pachayati raj: Introduction, PRI: Zila Pachayat. Elected officials and their roles, CEO Zila Pachayat: Position and role. Block level: Organizational Hierarchy(Different departments), Village level:Role of Elected and Appointed officials, Importance of grass root democracy.

UNIT VI ELECTION COMMISSION:
Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners - Institute and Bodies for the welfare of SC/ST/OBC and women.

TOTAL: 30 PERIODS

COURSE OUTCOMES

Students will be able to:

- Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
- Discuss the intellectual origins of the framework of argument that informed the conceptualization
- of social reforms leading to revolution in India.
- Discuss the circumstances surrounding the foundation of the Congress Socialist Party[CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
- Discuss the passage of the Hindu Code Bill of 1956.

SUGGESTED READING

1. The Constitution of India,1950(Bare Act),Government Publication.
2. Dr.S.N.Busi, Dr.B. R.Ambedkar framing of Indian Constitution,1st Edition, 2015.
3. M.P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis,2014.
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.

AX5096 PEDAGOGY STUDIES L T P C
2 0 0 0

OBJECTIVES

Students will be able to:

- Review existing evidence on there view topic to inform programme design and policy
- Making under taken by the DfID, other agencies and researchers.
- Identify critical evidence gaps to guide the development.

UNIT I INTRODUCTION AND METHODOLOGY:

Aims and rationale, Policy background, Conceptual framework and terminology - Theories of learning, Curriculum, Teacher education - Conceptual framework, Research questions **-** Overview of methodology and Searching.

UNIT II THEMATIC OVERVIEW

Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries - Curriculum, Teacher education.

UNIT III EVIDENCE ON THE EFFECTIVENESS OF PEDAGOGICAL PRACTICES

Methodology for the in depth stage: quality assessment of included studies - How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy? - Theory of change - Strength and nature of the body of evidence for effective pedagogical practices - Pedagogic theory and pedagogical approaches - Teachers' attitudes and beliefs and Pedagogic strategies.

UNIT IV PROFESSIONAL DEVELOPMENT

Professional development: alignment with classroom practices and follow up support - Peer support - Support from the head teacher and the community - Curriculum and assessment - Barriers to learning: limited resources and large class sizes

UNIT V RESEARCH GAPS AND FUTURE DIRECTIONS

Research design – Contexts – Pedagogy - Teacher education - Curriculum and assessment - Dissemination and research impact.

TOTAL: 30 PERIODS

COURSE OUTCOMES

Students will be able to understand:

- What pedagogical practices are being used by teachers informal and informal classrooms in developing countries?
- What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with what population of learners?
- How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?

SUGGESTED READING

1. Ackers J, HardmanF (2001) Classroom interaction in Kenyan primary schools, Compare, 31(2): 245-261.
2. Agrawal M (2004)Curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies, 36(3):361-379.
3. Akyeampong K (2003) Teacher training in Ghana-does it count? Multi-site teacher education research project (MUSTER) country report 1.London:DFID.
4. Akyeampong K, Lussier K, Pryor J, Westbrook J (2013) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? International Journal Educational Development, 33(3): 272–282.
5. Alexander RJ(2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell.
6. Chavan M(2003) Read India: Amass scale, rapid, 'learning to read' campaign.
7. www.pratham.org/images/resource%20working%20paper%202.pdf

AX5097 **STRESS MANAGEMENT BY YOGA** **L T P C**
2 0 0 0

OBJECTIVES

- To achieve overall health of body and mind
- To overcome stress

UNIT I

Definitions of Eight parts of yoga.(Ashtanga)

UNIT II

Yam and Niyam - Do`s and Don't's in life - i) Ahinsa, satya, astheya, bramhacharya and aparigraha, ii) Ahinsa, satya, astheya, bramhacharya and aparigraha.

UNIT III

Asan and Pranayam - Various yog poses and their benefits for mind & body - Regularization of breathing techniques and its effects-Types of pranayam

TOTAL: 30 PERIODS

OUTCOMES

Students will be able to:

- Develop healthy mind in a healthy body thus improving social health also
- Improve efficiency

SUGGESTED READING

1. 'Yogic Asanas for Group Tarining-Part-I":Janardan Swami Yoga bhyasi Mandal, Nagpur
2. "Rajayoga or conquering the Internal Nature" by Swami Vivekananda, Advaita Ashrama (Publication Department), Kolkata

AX5098 **PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS** **L T P C**
2 0 0 0

OBJECTIVES

- To learn to achieve the highest goal happily
- To become a person with stable mind, pleasing personality and determination
- To awaken wisdom in students

UNIT I

Neetisatakam-holistic development of personality - Verses- 19,20,21,22 (wisdom) - Verses-29,31,32 (pride & heroism) – Verses- 26,28,63,65 (virtue) - Verses- 52,53,59 (dont's) - Verses-71,73,75,78 (do's)

UNIT II

Approach to day to day work and duties - Shrimad Bhagwad Geeta: Chapter 2-Verses 41, 47,48 - Chapter 3-Verses 13, 21, 27, 35 Chapter 6-Verses 5,13,17,23, 35 - Chapter 18-Verses 45, 46, 48.

UNIT III

Statements of basic knowledge - Shrimad Bhagwad Geeta: Chapter2-Verses 56, 62, 68 Chapter 12 -Verses 13, 14, 15, 16,17, 18 - Personality of role model - shrimad bhagwad geeta - Chapter2-Verses 17, Chapter 3-Verses 36,37,42 - Chapter 4-Verses 18, 38,39 Chapter18 – Verses 37,38,63

TOTAL: 30 PERIODS

COURSE OUTCOMES

Students will be able to

- Study of Shrimad-Bhagwad-Geeta will help the student in developing his personality and achieve the highest goal in life
- The person who has studied Geeta will lead the nation and mankind to peace and prosperity
- Study of Neet is hatakam will help in developing versatile personality of students.

SUGGESTED READING

1. Gopinath, Rashtriya Sanskrit Sansthanam P, Bhartrihari's Three Satakam, Niti-sringar-vairagya, New Delhi,2010
2. Swami Swarupananda , Srimad Bhagavad Gita, Advaita Ashram, Publication Department, Kolkata, 2016.